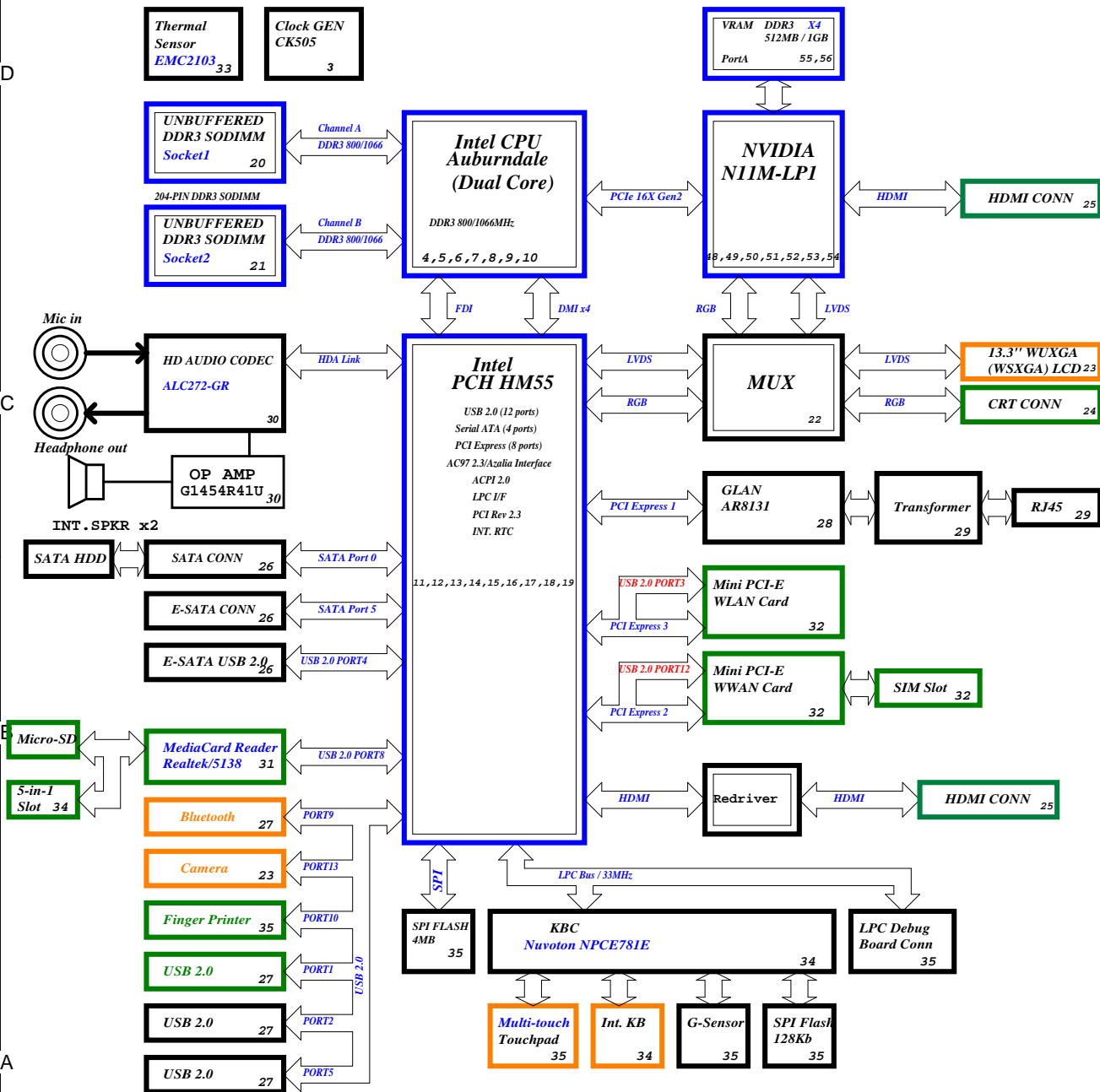


LA36 Switchable Graphics System Schematics

Project Code: 91.4JG01.001
PCB(Raw Card): 09939-1

PCB LAYER

L1: Top
L2: VCC/GND
L3: Signal
L4: Signal
L5: GND
L6: Boot



Finger Printer BD

BT BD

AV BD

CPU DC/DC
ISL62882 40, 41

INPUTS	OUTPUTS
DCBATOUT	VCC_CORE

SYSTEM DC/DC
RT8223BGQW 42

INPUTS	OUTPUTS
DCBATOUT	5V_AUX_S5 3D3V_AUX_S5 5V_S5 3D3V_S5

SYSTEM DC/DC
RT8209E 44

INPUTS	OUTPUTS
DCBATOUT	1D5V_S3

SYSTEM DC/DC
RT8209E 44

INPUTS	OUTPUTS
DCBATOUT	1D05V_S0

SYSTEM DC/DC
RT8209E 45

INPUTS	OUTPUTS
DCBATOUT	1D05V_VTT

LDO
RT9025 46

INPUTS	OUTPUTS
3D3V_S5	1D8V_S0

LDO
RT9026 46

INPUTS	OUTPUTS
1D5V_S3	0D75_S0 DDR_VREF_S3

SYSTEM DC/DC
ISL62881 47

INPUTS	OUTPUTS
DCBATOUT	VCC_GFXCORE

SYSTEM DC/DC
RT8208A 45

INPUTS	OUTPUTS
DCBATOUT	VGA_CORE_S0

CHARGER
BQ24745 43

INPUTS	OUTPUTS
DCBATOUT	BT+

<Variant Name>

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Taipei Hsein 221, Taiwan, R.O.C

Title	Block Diagram	Rev
Size	Document Number	LA36 MB
Customer		-1
Date	Monday, March 22, 2010	Sheet 1 of 58

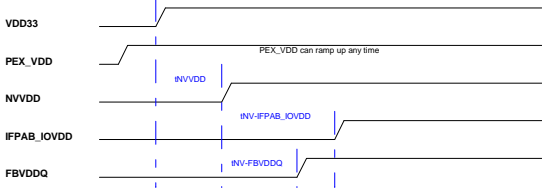
Processor Strapping

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[4]	Embedded DisplayPort Presence	1: Disabled - No Physical Display Port attached to Embedded DisplayPort. 0: Enabled - An external Display Port device is connected to the Embedded Display Port.	1
CFG[3]	PCI-Express Static Lane Reversal	1: Normal Operation. 0: Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	1
CFG[0]	PCI-Express Configuration Select	1: Single PCI-Express Graphics 0: Bifurcation enabled	1
CFG[7]	Reserved - Temporarily used for early Clarkfield samples.	Clarkfield (only for early samples pre-ES1) - Connect to GND with 3.01K Ohm/5% resistor Note: Only temporary for early CFD samples (rPDK/BGA) [For details please refer to the WW33 MoW and sighting report]. For a common motherboard design (for AUB and CFD), the pull-down resistor should be used. Does not impact AUB functionality.	0

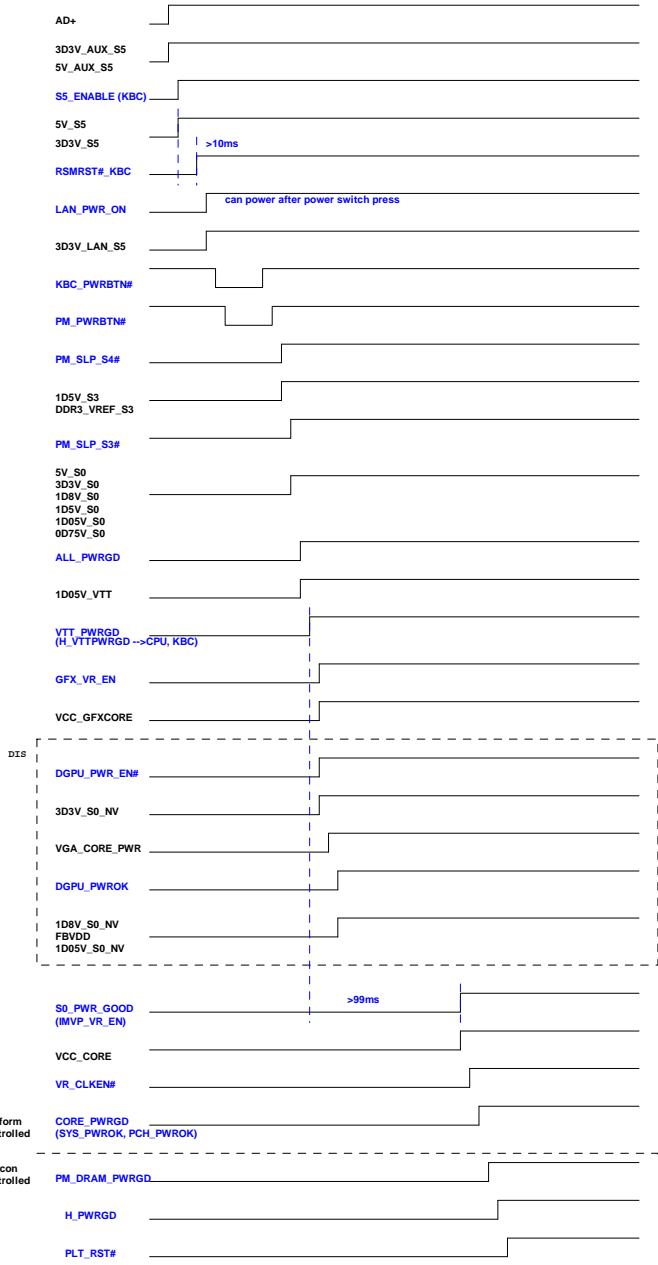
PCH Strapping

Name	Schematics Notes
SPKR	Reboot option at power-up Default Mode: Internal weak Pull-down. No Reboot Mode with TCO Disabled: Connect to Vcc3_3 with 8.2-kΩ - 10-kΩ weak pull-up resistor.
INIT3_3V#	Weak internal pull-down. Do not pull high.
GNT3#/GPIO55	Default Mode: Internal pull-up. Low (0) = Top Block Swap Mode (Connect to ground with 4.7-kΩ weak pull-down resistor).
INTVMEN	High (1) = Integrated VRM is enabled Low (0) = Integrated VRM is disabled
GNT0#, GNT1#	Default (SPI): Left both GNT0# and GNT1# floating. No pull up required. Boot from PCI: Connect GNT1# to ground with 1-kΩ pull-down resistor. Leave GNT0# Floating. Boot from LPC: Connect both GNT0# and GNT1# to ground with 1-kΩ pull-down resistor.
GNT2#/GPIO53	Default - Internal pull-up. Low (0)= Configures DMI for ESI compatible operation (for servers only. Not for mobile/desktops).
GPIO33	Default: Do not pull low. Disable ME in Manufacturing Mode: Connect to ground with 1-kΩ pull-down resistor.
SPI_MOSI	Enable iTPM: Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor Disable iTPM: Left floating, no pull-down required.
NV_ALE	Enable Danbury: Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor. Disable Danbury: Connect to ground with 4.7-kΩ weak pull-down resistor.
NC_CLE	Weak internal pull-up. Do not pull low.
HAD_DOCK_EN#/GPIO[33]	Low (0): Flash Descriptor Security will be overridden. High (1) : Flash Descriptor Security will be in effect.
HDA_SDO	Weak internal pull-down. Do not pull high.
HDA_SYNC	Weak internal pull-down. Do not pull high.
GPIO15	Weak internal pull-down. Do not pull high.
GPIO8	Weak internal pull-up. Do not pull low.
GPIO27	Default = Do not connect (floating) High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

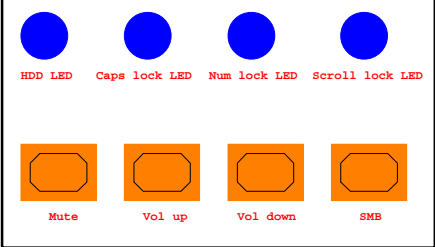
N11M-GE Power Sequence



Sequence AC

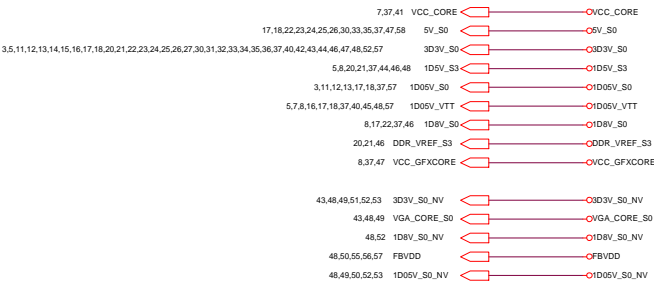


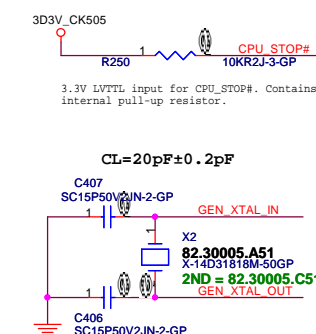
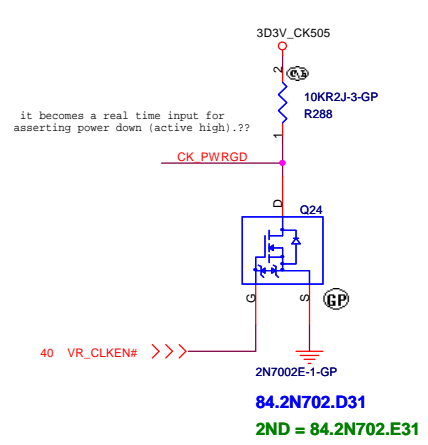
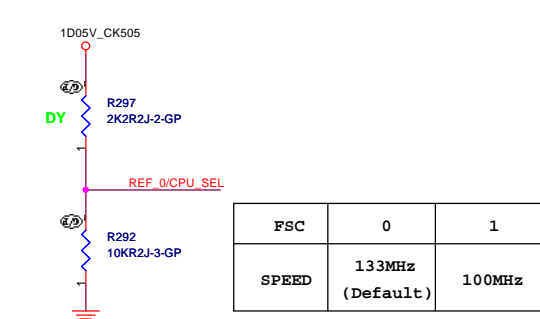
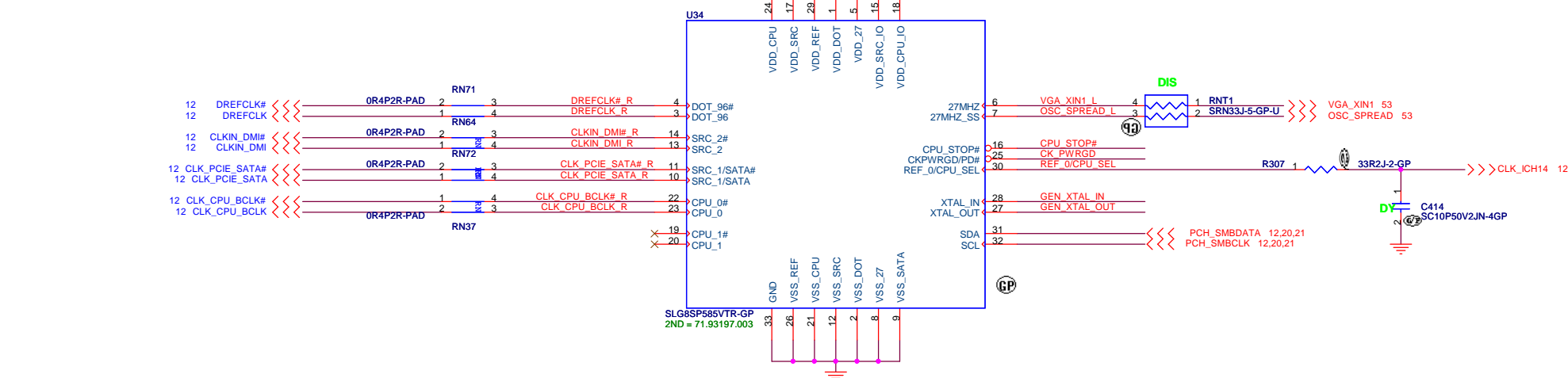
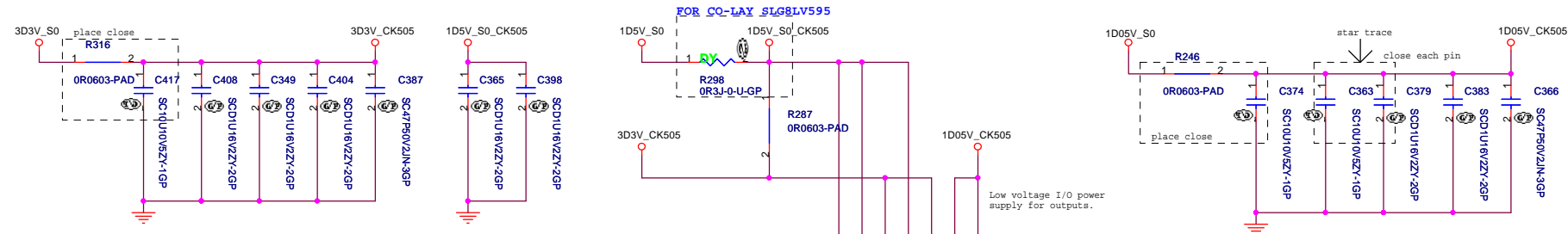
AV PANEL



PLANAR_ID[1..0]

KBC GPin	31	23	Planar ID Version	Planar PCB Version
PLANAR_IDn	1	0		
	0	0	LA36 - SA	SA
	0	1		SB
	1	0		SC
	1	1		-1

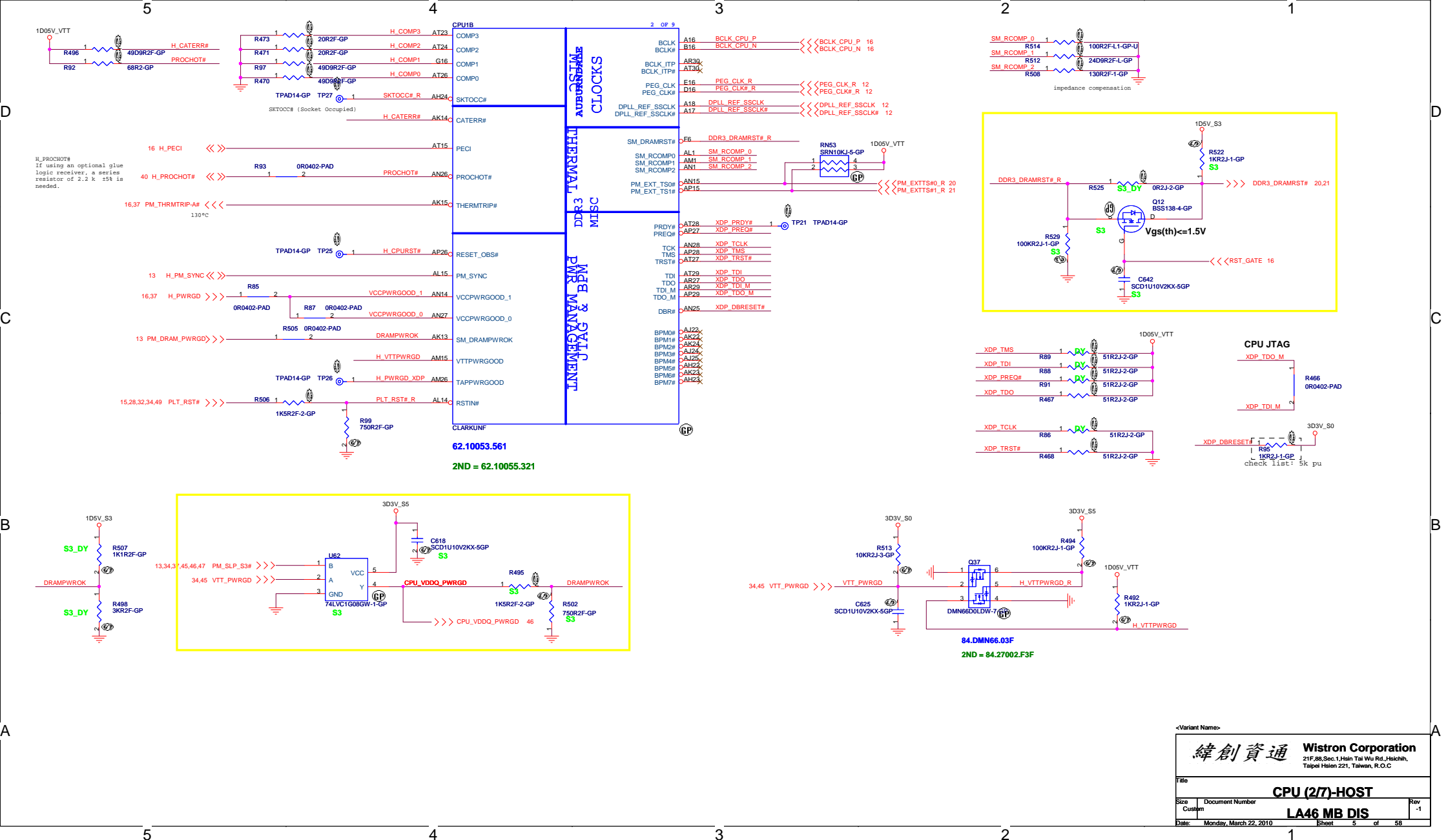


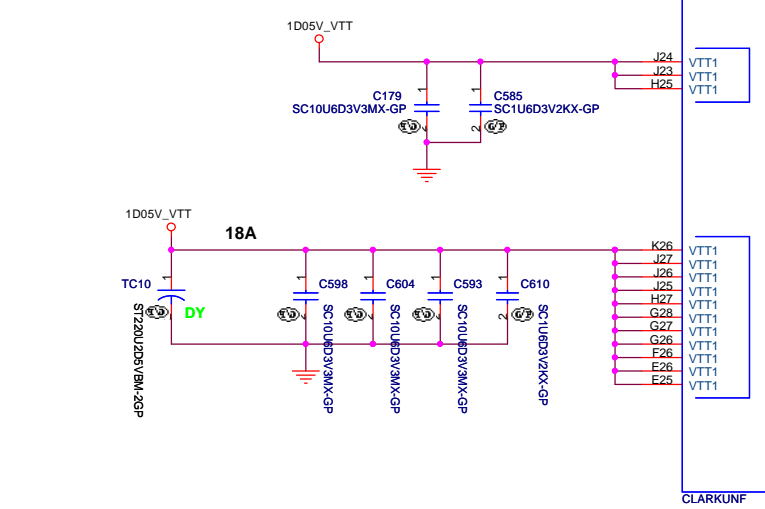
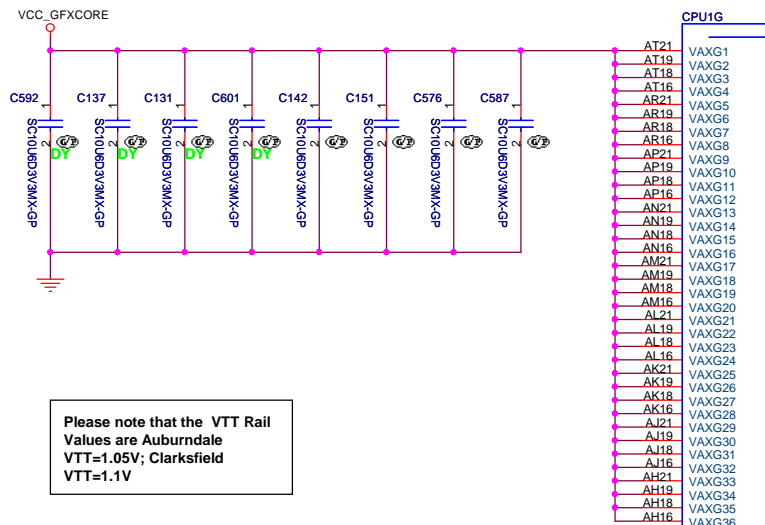


Layout Notes:

Make sure that the stubs to the test points(CK_PWRGD, CLK_EN#, GEN_XTAL_OUT) in the layout are as short as possible on the high speed signals.



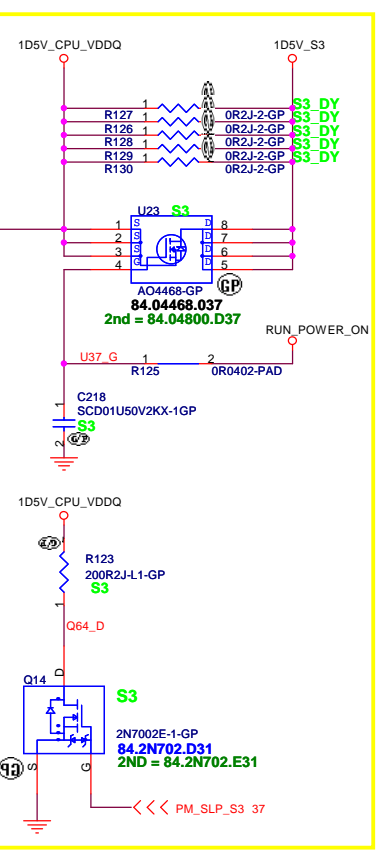
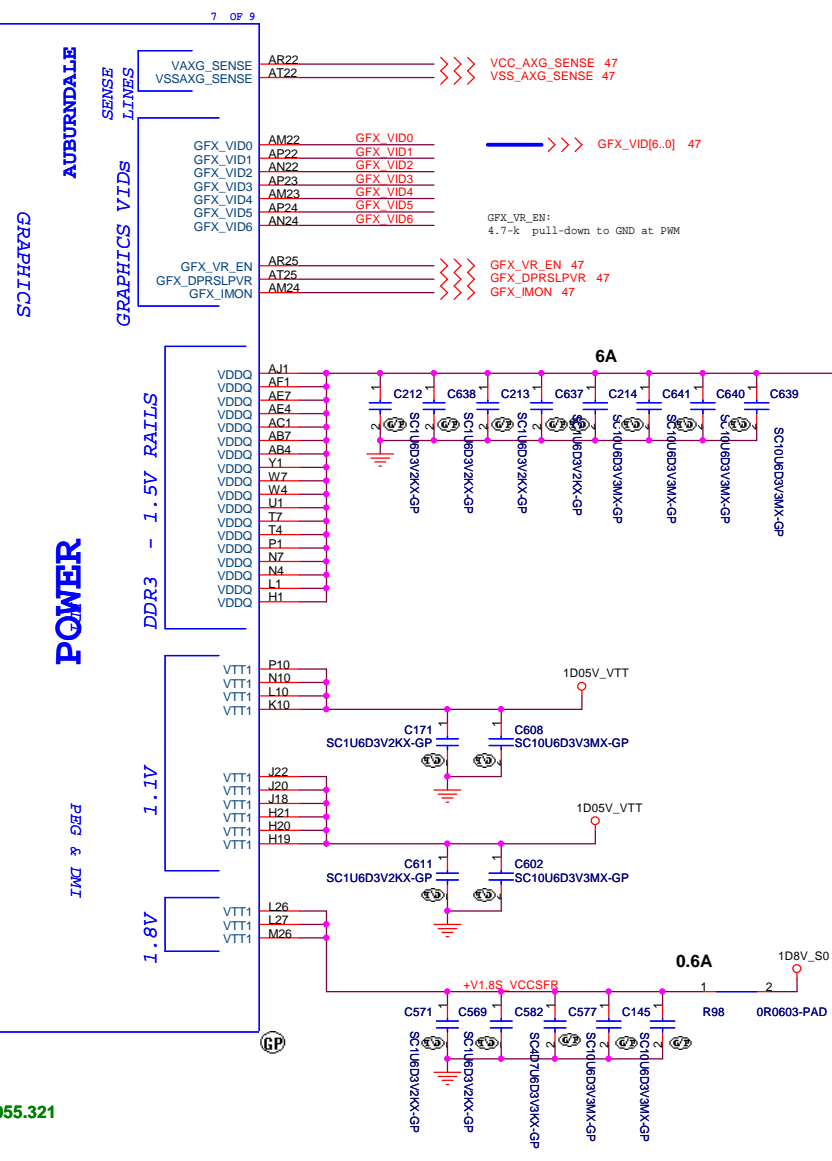


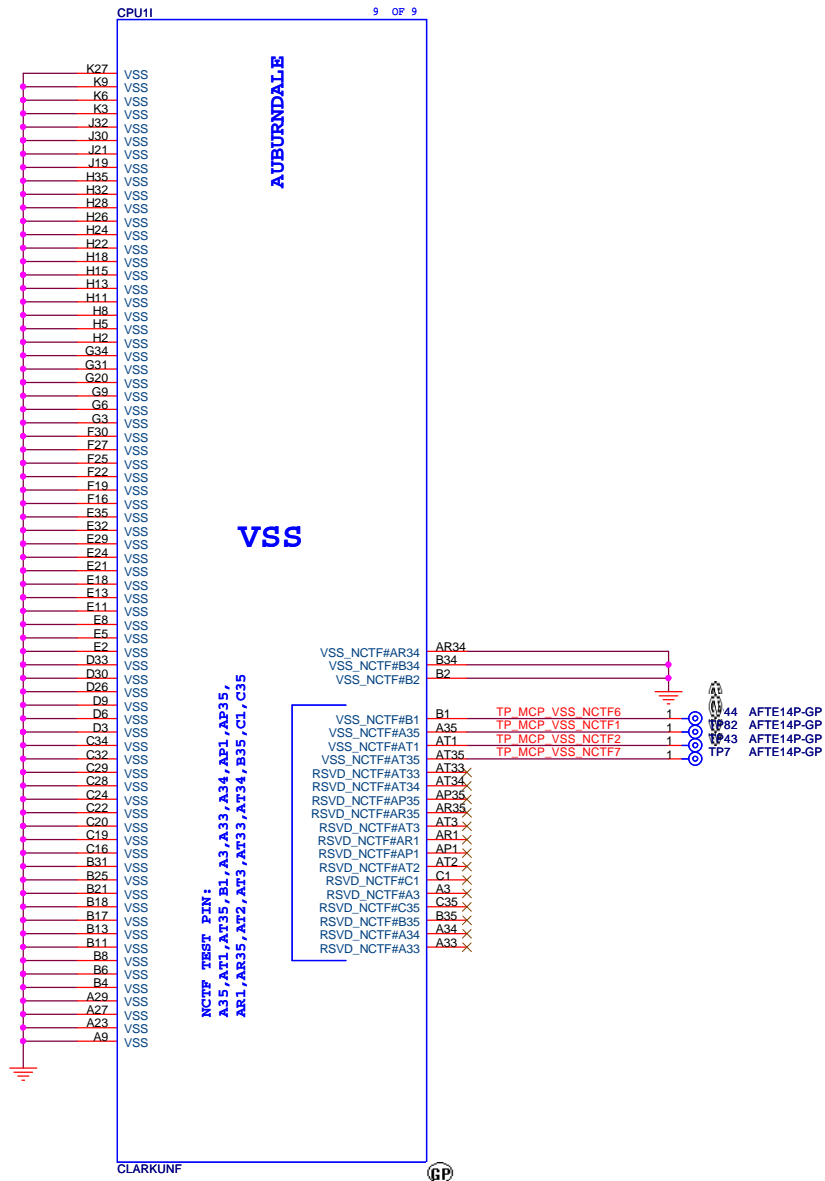
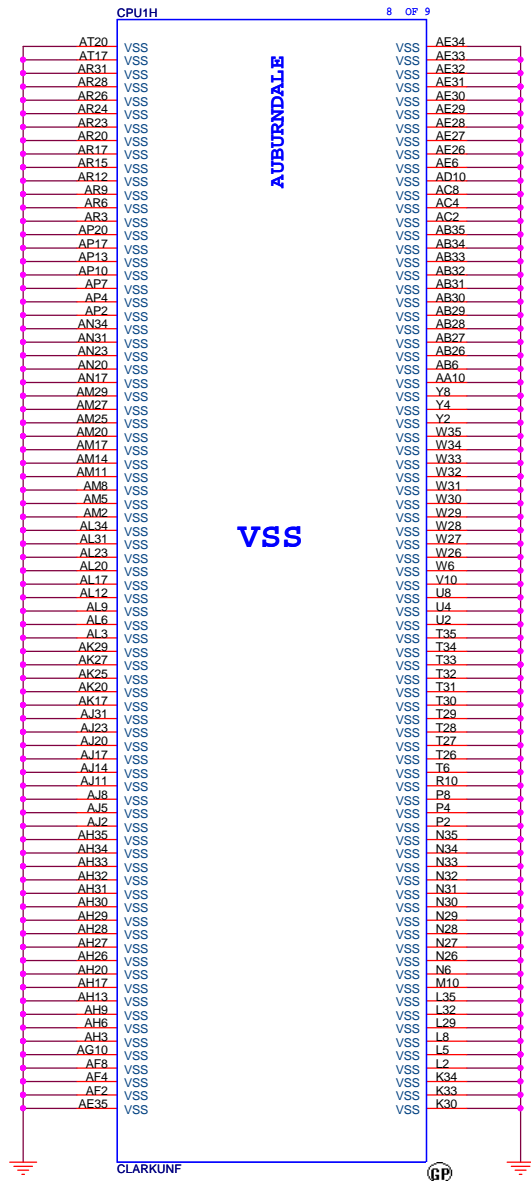


CLARKKUNF

62.10053.561

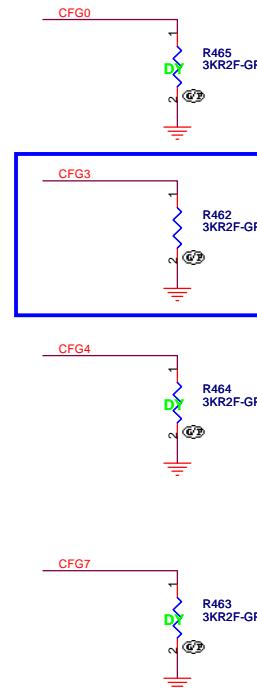
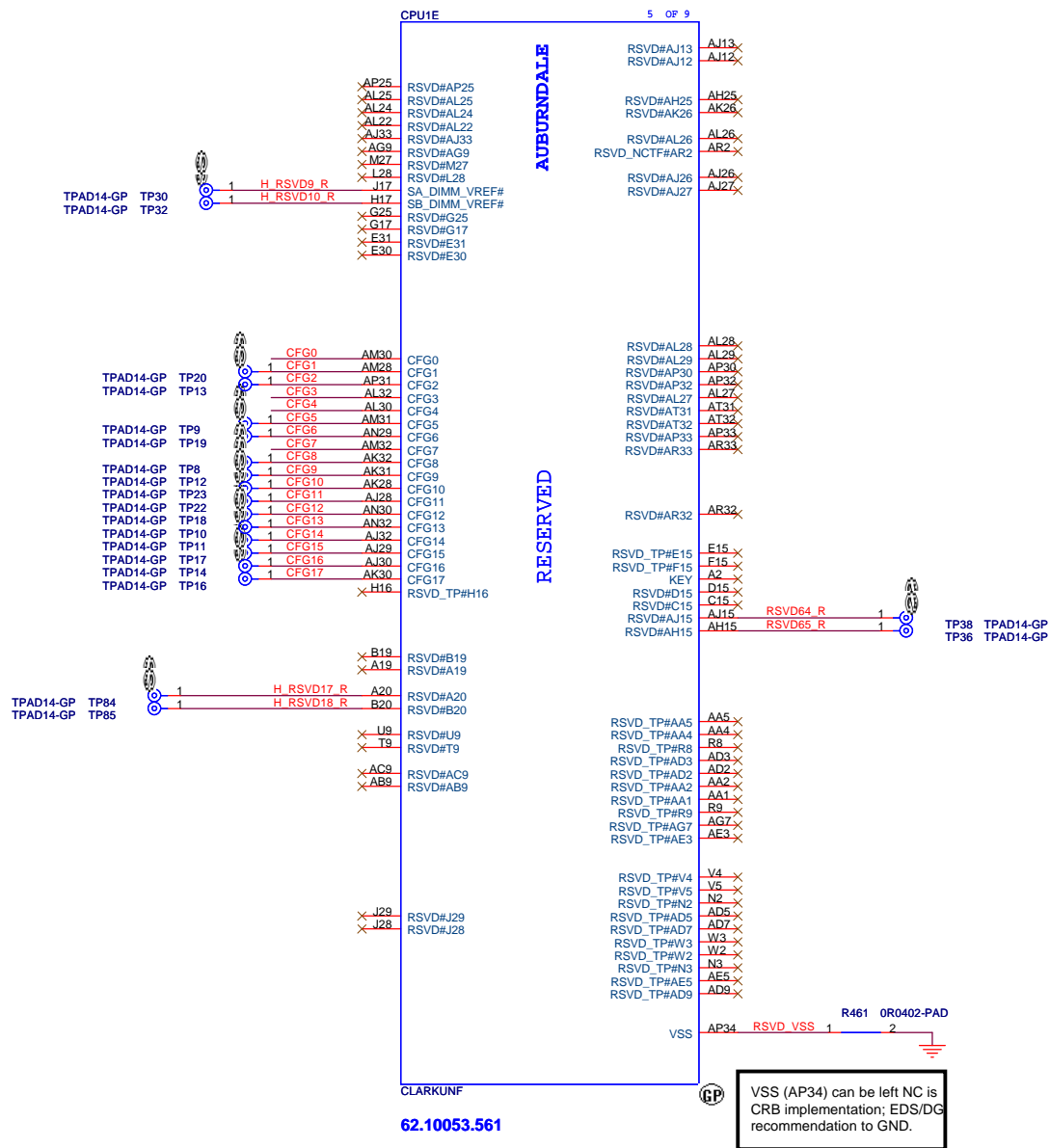
2ND = 62.10055.321





<Variant Name>

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Title	
CPU (6/7)-VSS	
Size A3	Document Number LA36 MB DIS
Date: Monday, March 22, 2010	Sheet 9 of 58
Rev -1	



PCI-Express Configuration Select	
CFG0	1:Single PEG 0:Bifurcation enabled

CFG3 - PCI-Express Static Lane Reversal	
CFG3	1 :Normal Operation 0 :Lane Numbers Reversed 15 -> 0, 14 -> 1, ...

CFG4 - Display Port Presence	
CFG4	1:Disabled; No Physical Display Port attached to Embedded Display Port 0:Enabled; An external Display Port device is connected to the Embedded Display Port

CFG7(Reserved) - Temporarily used for early Clarksfield samples.	
CFG7	Clarksfield (only for early samples pre-ES1) - Connect to GND with 3.01K Ohm/5% resistor. Note: Only temporary for early CFD sample (rPGA/BGA) [For details please refer to the WW33 MoW and sighting report]. For a common M/B design (for AUB and CFD), the pull-down resistor should be used. Does not impact AUB functionality.

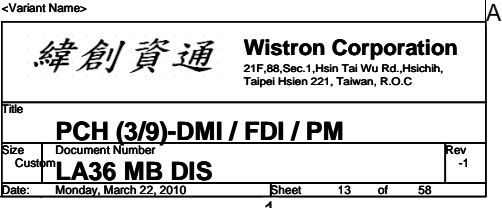
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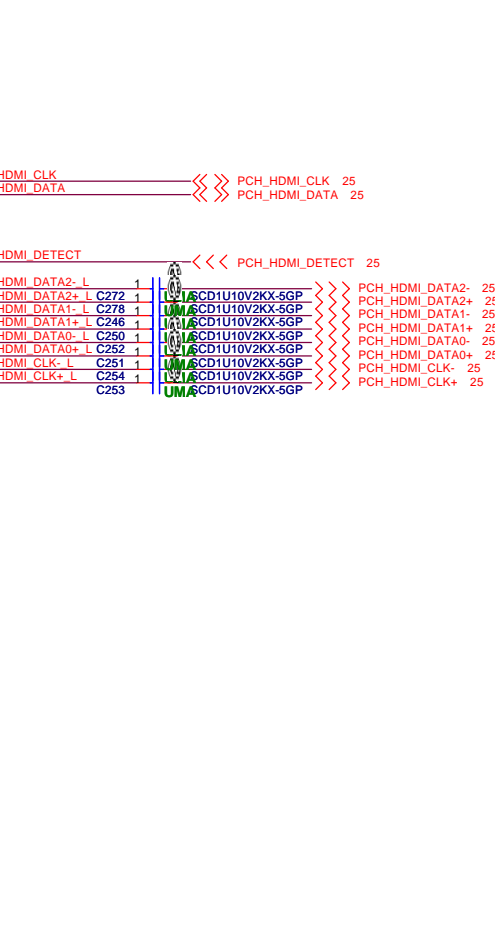
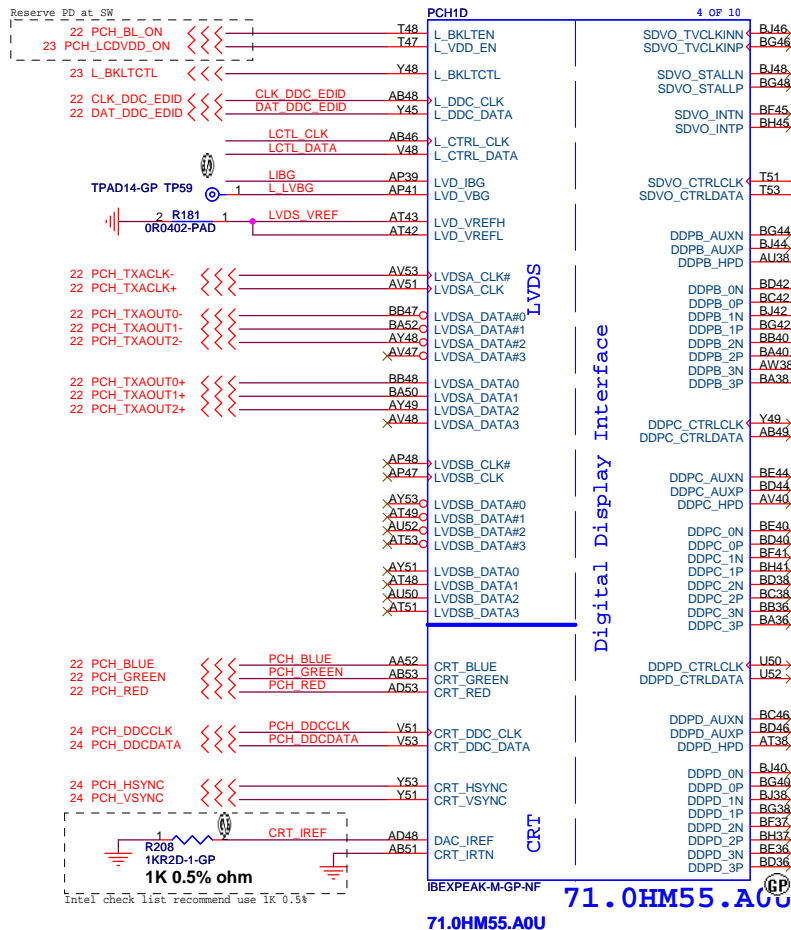
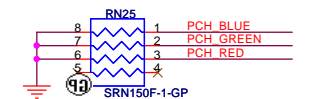
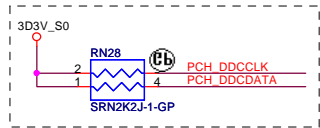
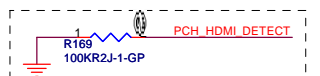
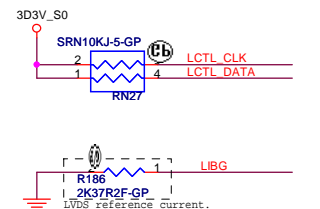
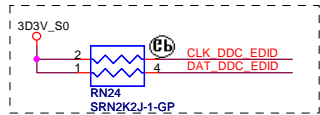
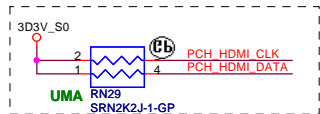
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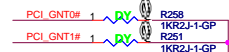
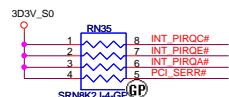
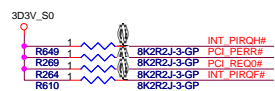
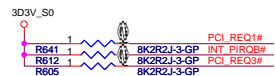
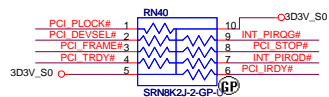
Title		CPU (777)-RESERVED	
Size	A3	Document Number	LA36 MB DIS
Date:	Monday, March 22, 2010	Sheet	10 of 58

Rev -1

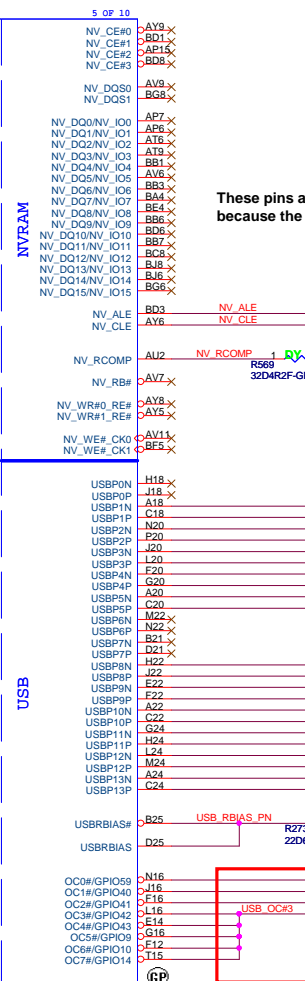
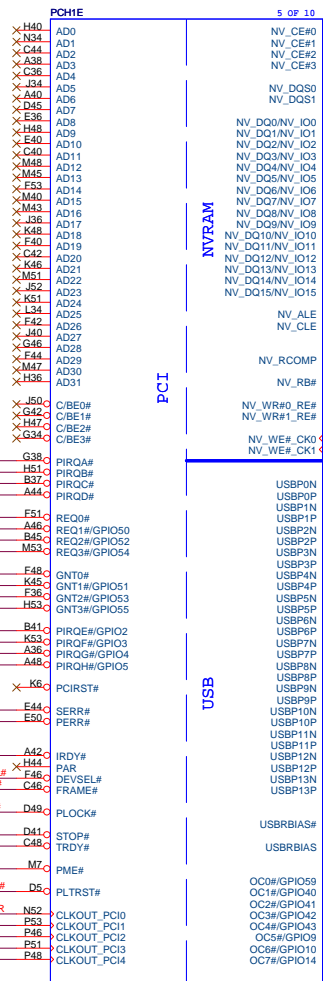
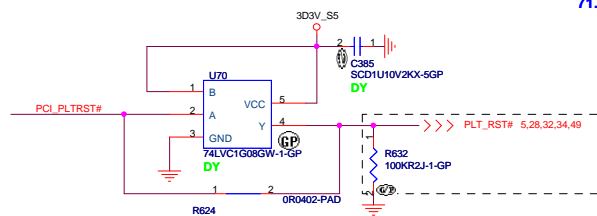
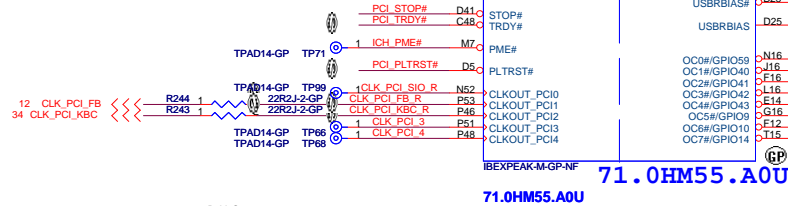
3



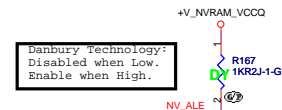
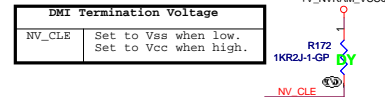




BOOT BIOS Strap		
PCI_GNT#0	PCI_GNT#1	BOOT BIOS Location
0	0	LPC
1	0	Reserved
0	1	PCI
1	1	SPI(Default)

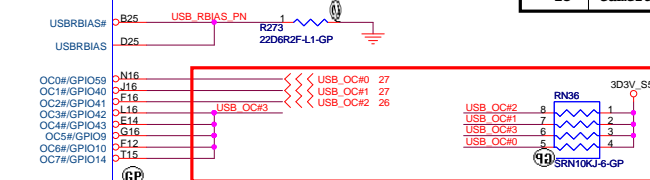


These pins are left as NC,
because the function is disable.



CHECK

Pair	Device
0	NC
1	USB3
2	USB1
3	WLAN
4	E-SATA
5	USB2
6	Disable (HM55)
7	Disable (HM55)
8	Card Reader
9	Blue Tooth
10	Finger Print
11	Micro SD
12	WWAN
13	Camera

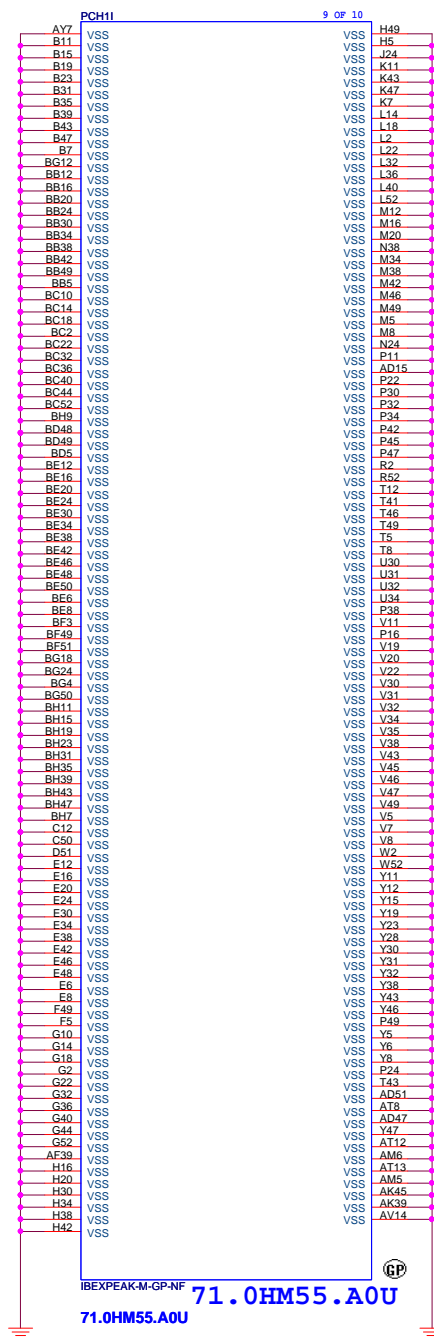
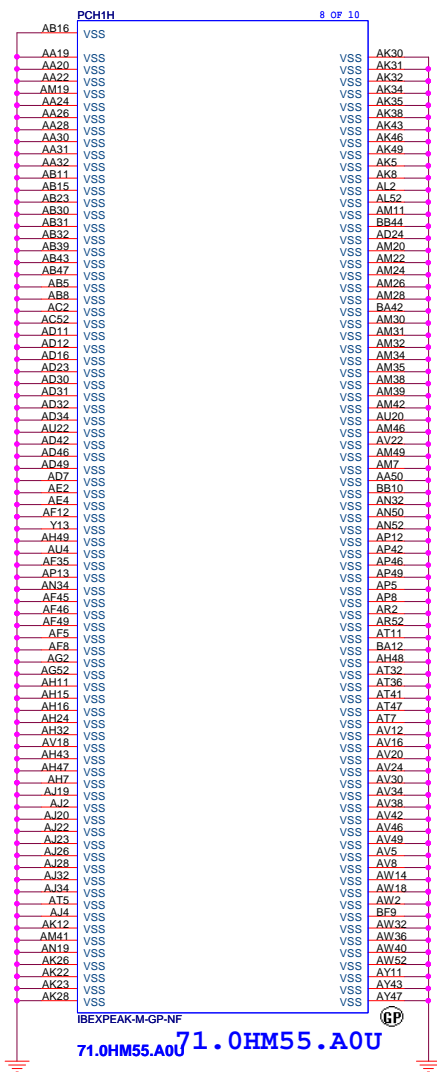


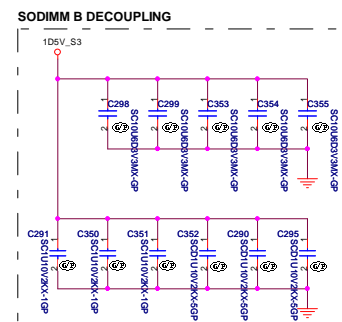
OC#0	Port 0 & 1	EHCI
OC#1	Port 2 & 3	
OC#2	Port 4 & 5	
OC#3	Port 6 & 7	
OC#4	Port 8 & 9	EHCI
OC#5	Port 10 & 11	
OC#6	Port 12 & 13	
OC#7	Floater OC# (not used)	

<Variant Name>

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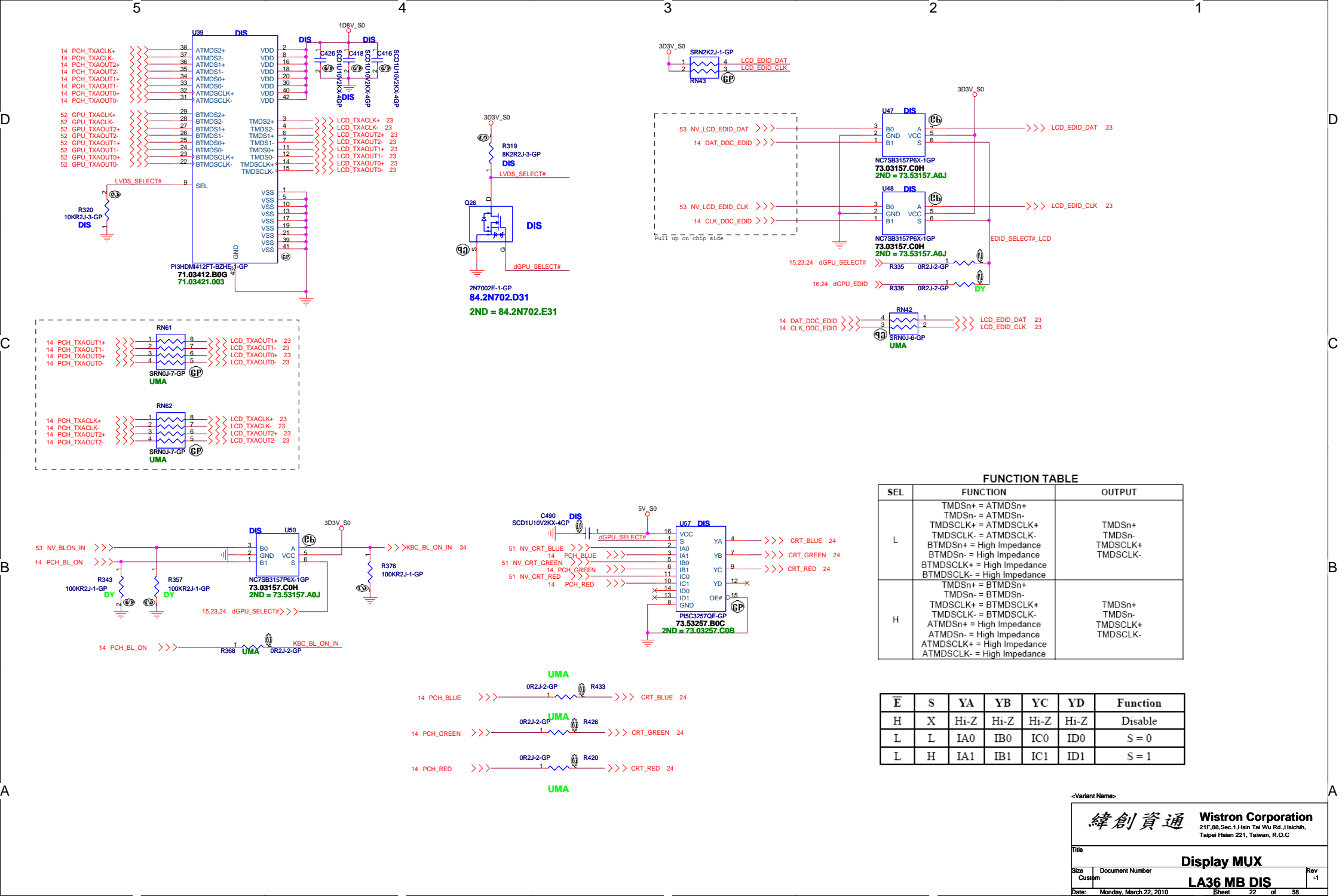
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Size	Document Number	Rev	
Custom	LA36 MB DIS		
Date: Monday, March 22, 2010	Sheet 15	of 58	



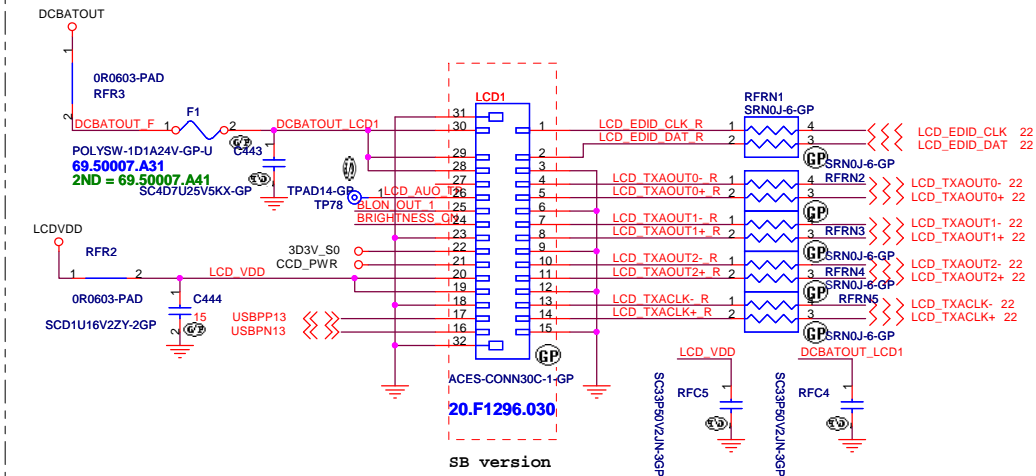


H = 8mm

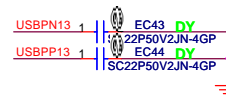
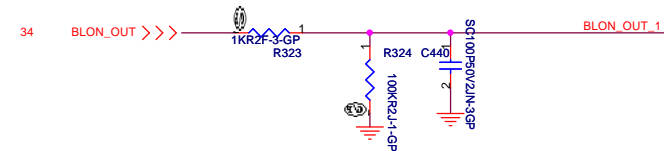
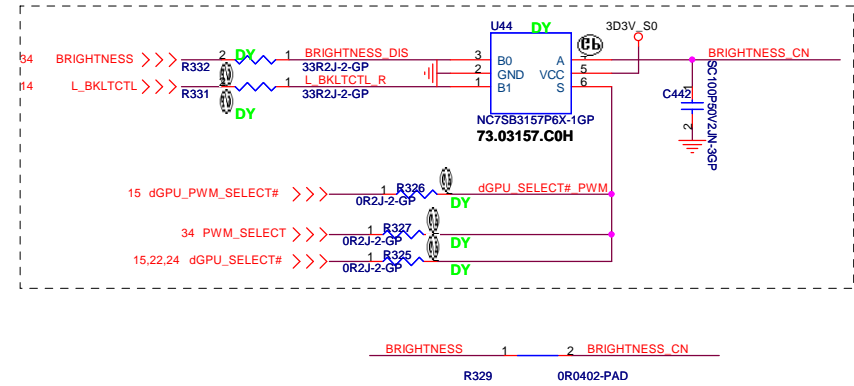
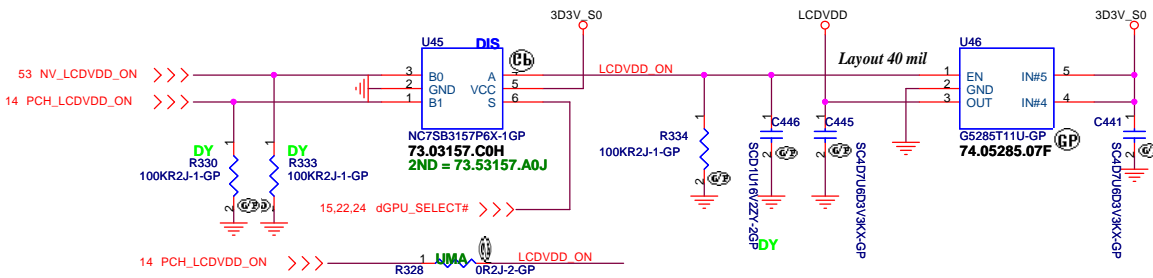
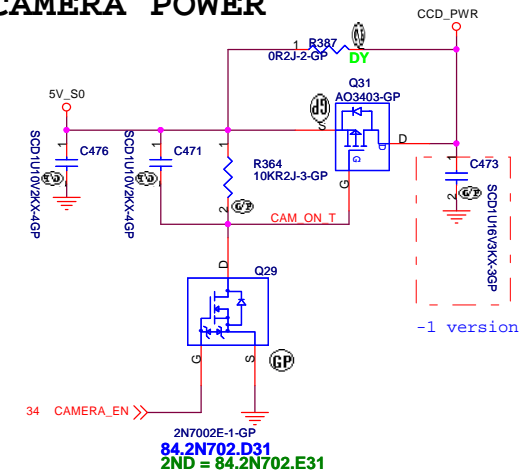
SO-DIMMB is placed farther from the Processor than SO-DIMMA



LCD/INVERTER/CCD CONN



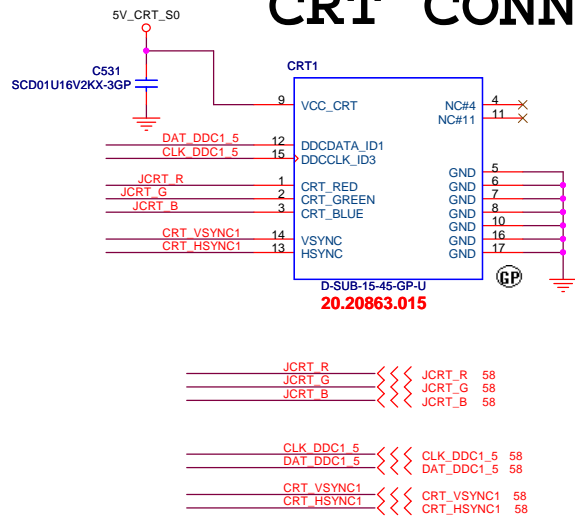
CAMERA POWER



<Variant Name>

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21F, 88, Sec. 1, Heil Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C			
Title			
LCD & CCD			
Size	Document Number	Rev	
A3	LA36 MB DIS	-1	
Date:	Monday, March 22, 2010	Sheet	23 of 58

CRT CONN



L=>B0 -DIS
H=>B1 -UMA

15,22,23 dGPU_SELECT#

For DIS CRT

51 NV_CRT_HSYNC

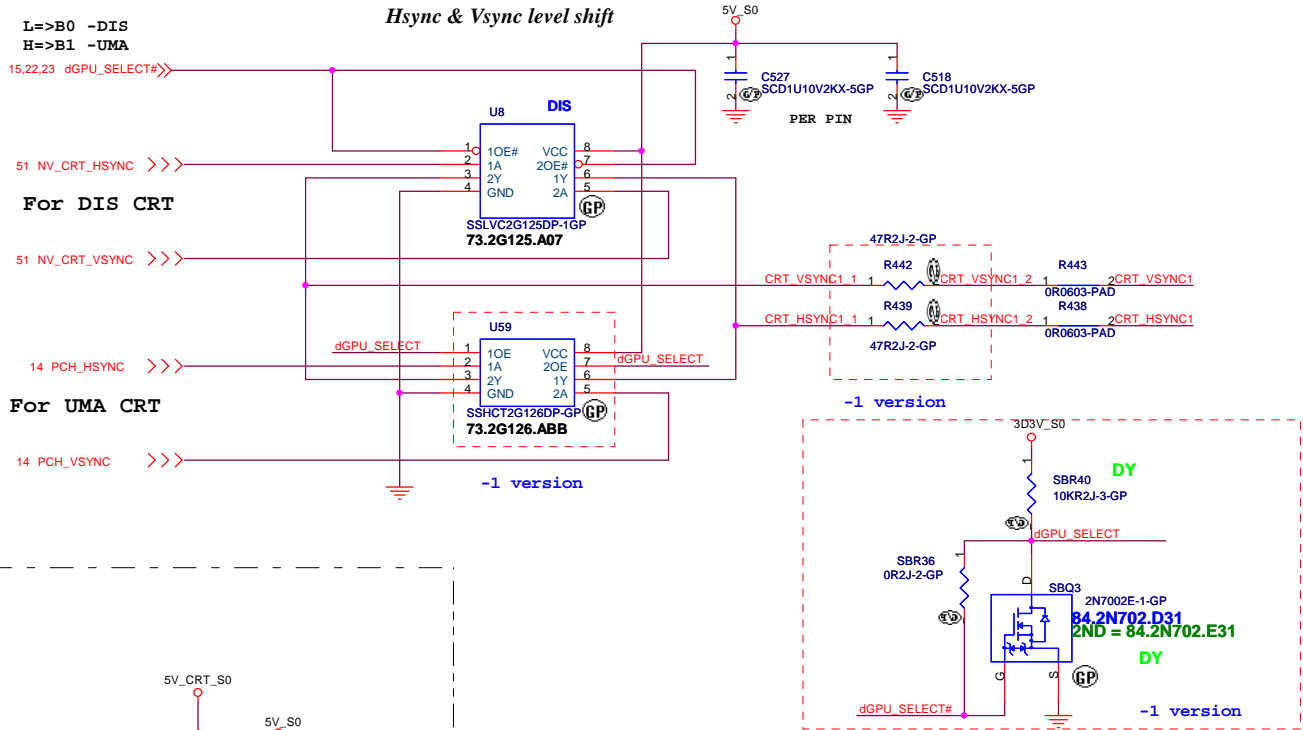
51 NV_CRT_VSYNC

For UMA CRT

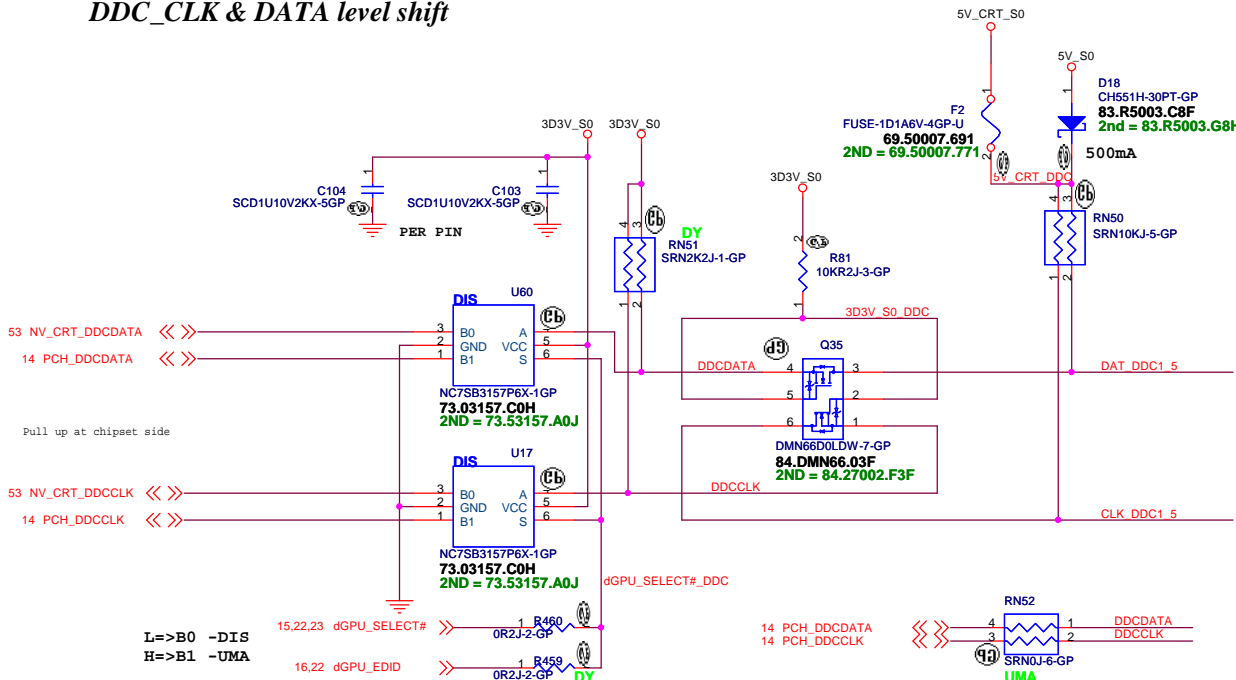
14 PCH_HSYNC

14 PCH_VSYNC

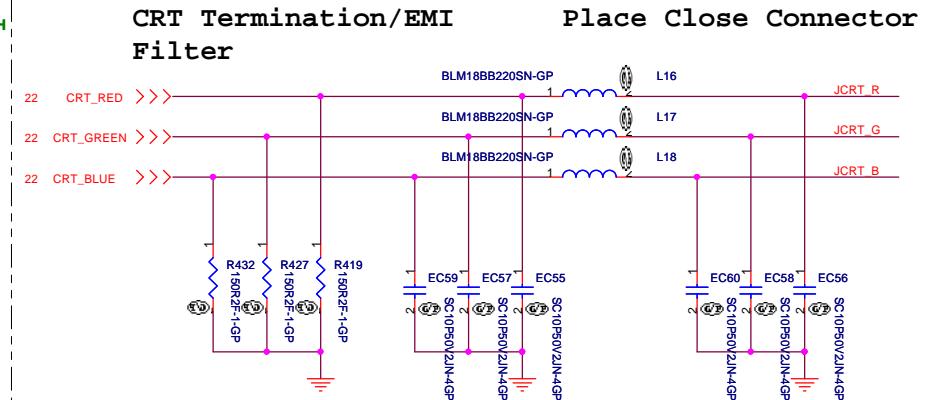
Hsync & Vsync level shift



DDC_CLK & DATA level shift



CRT Termination/EMI Filter



Place Close Connector

<Variant Name>

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Taipei Hsien 221, Taiwan, R.O.C

Title

CRT

Size

A3

Document Number

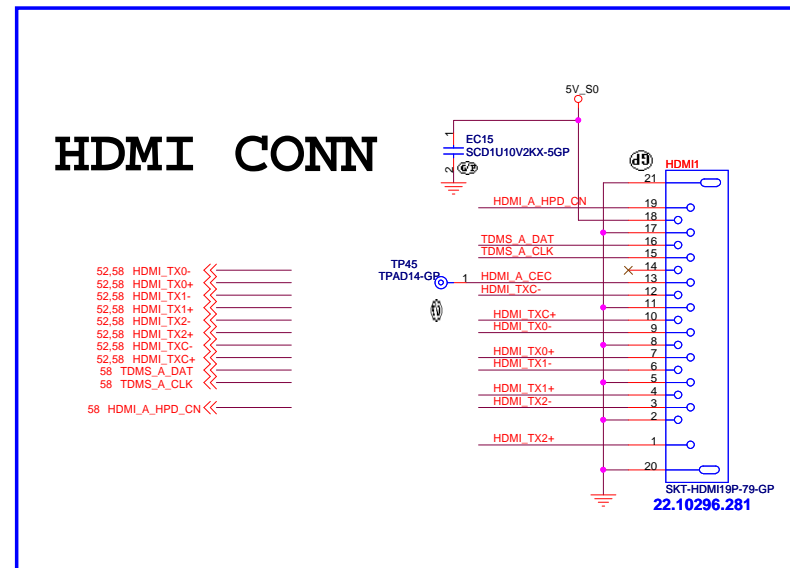
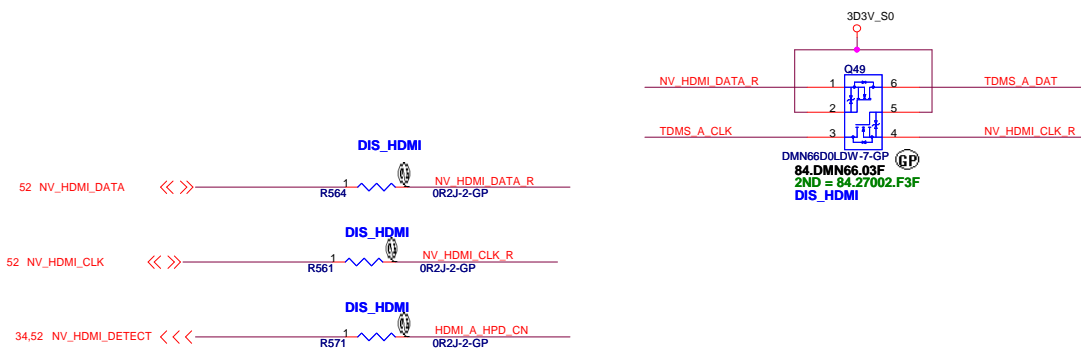
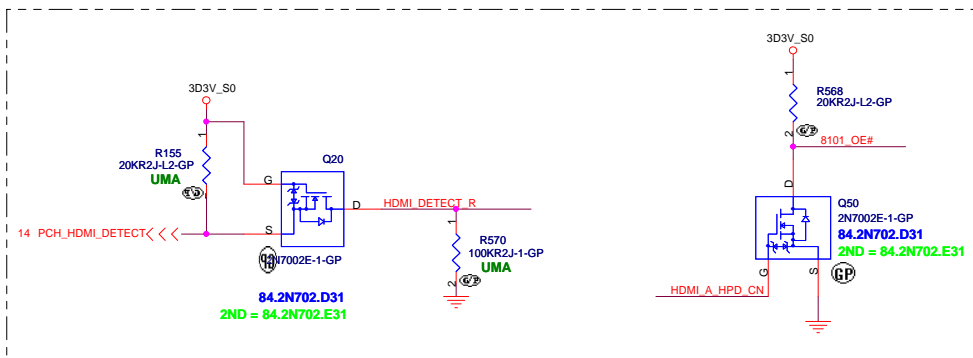
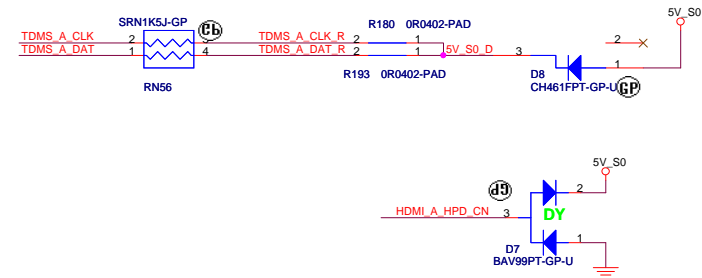
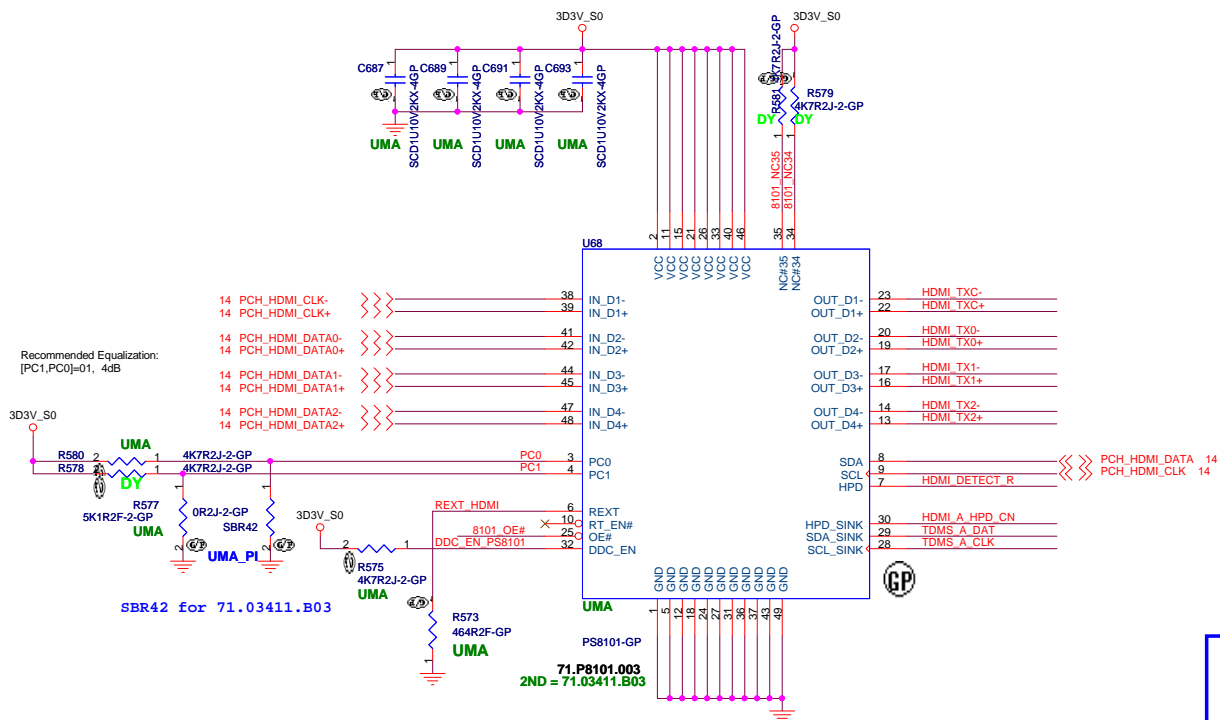
LA36 MB DIS

Date: Monday, March 22, 2010

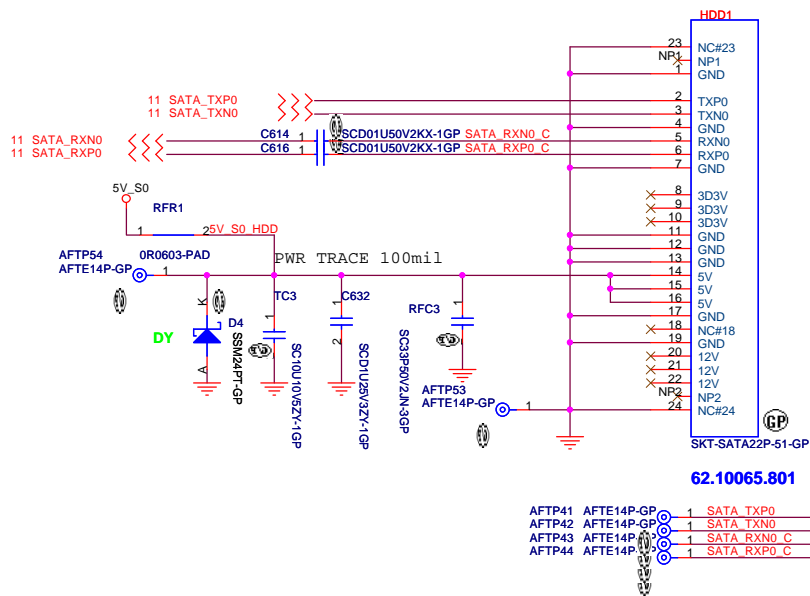
Sheet 24 of 58

Rev

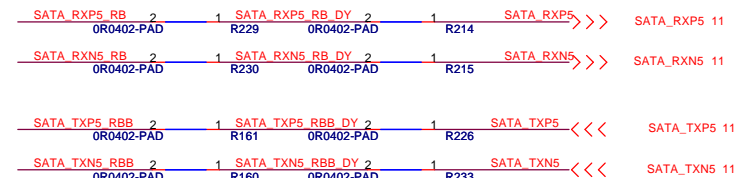
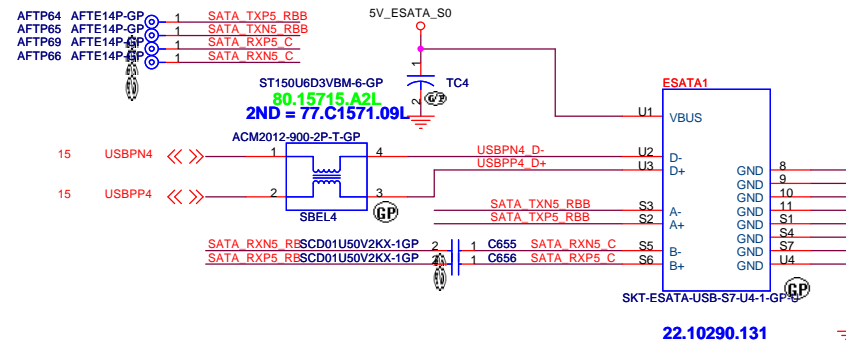
-1



SATA Connector

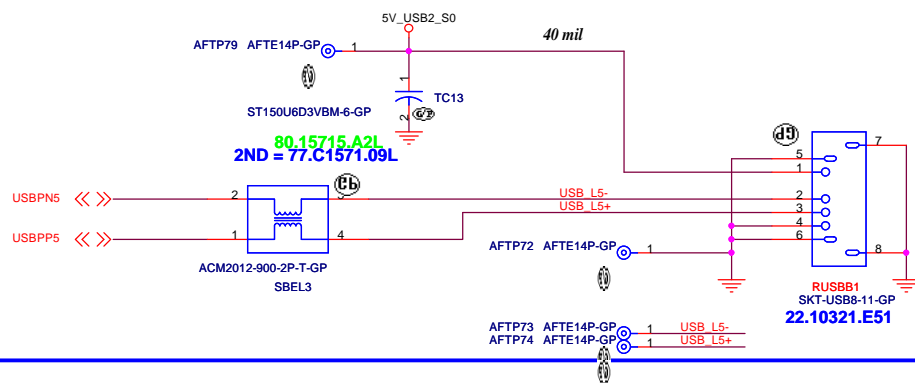


E-SATA Connector

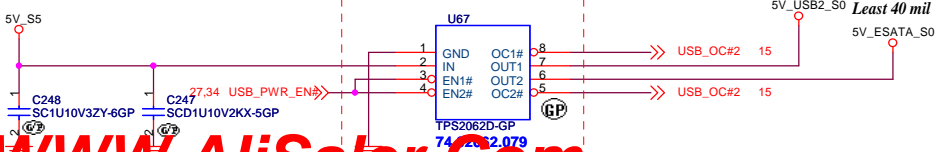


-1 Version

USB2



-1 version

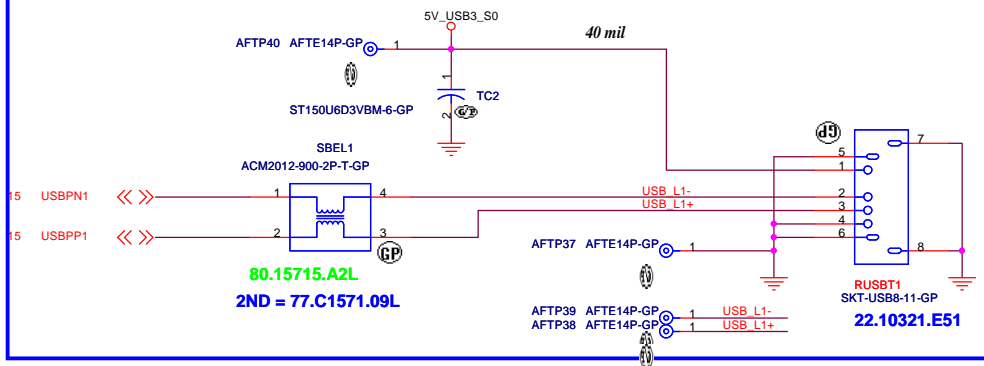


<Variant Name>

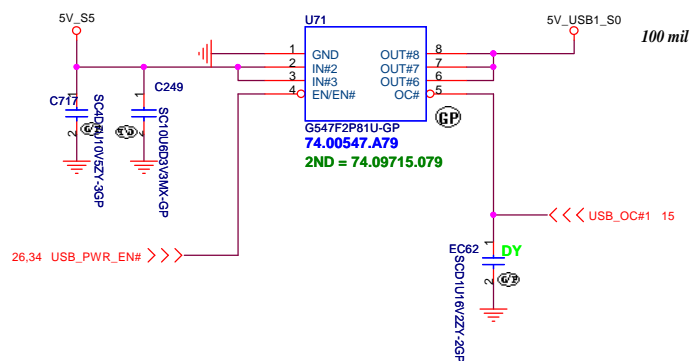
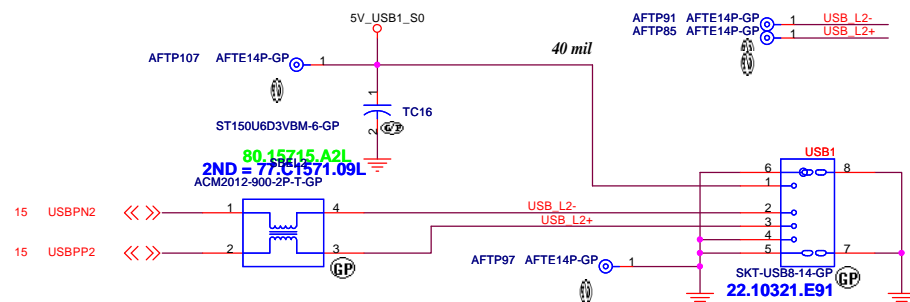
緯創資通 Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C

Title		
HDD & E-SATA&USB2		
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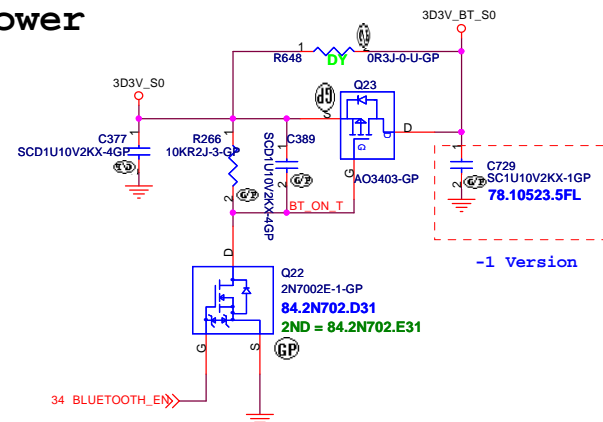
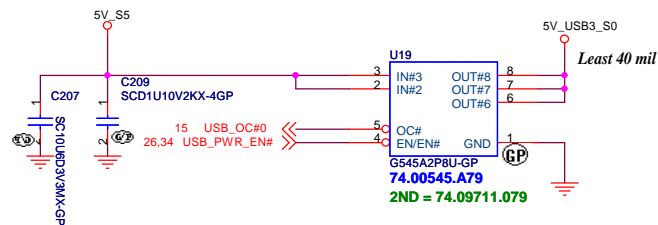
USB3



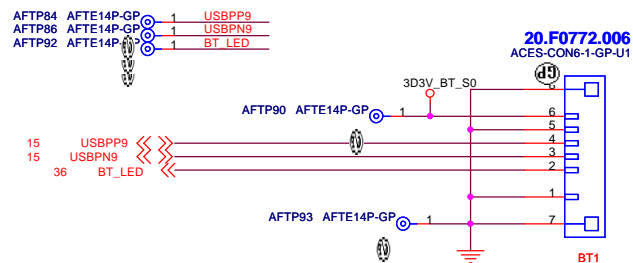
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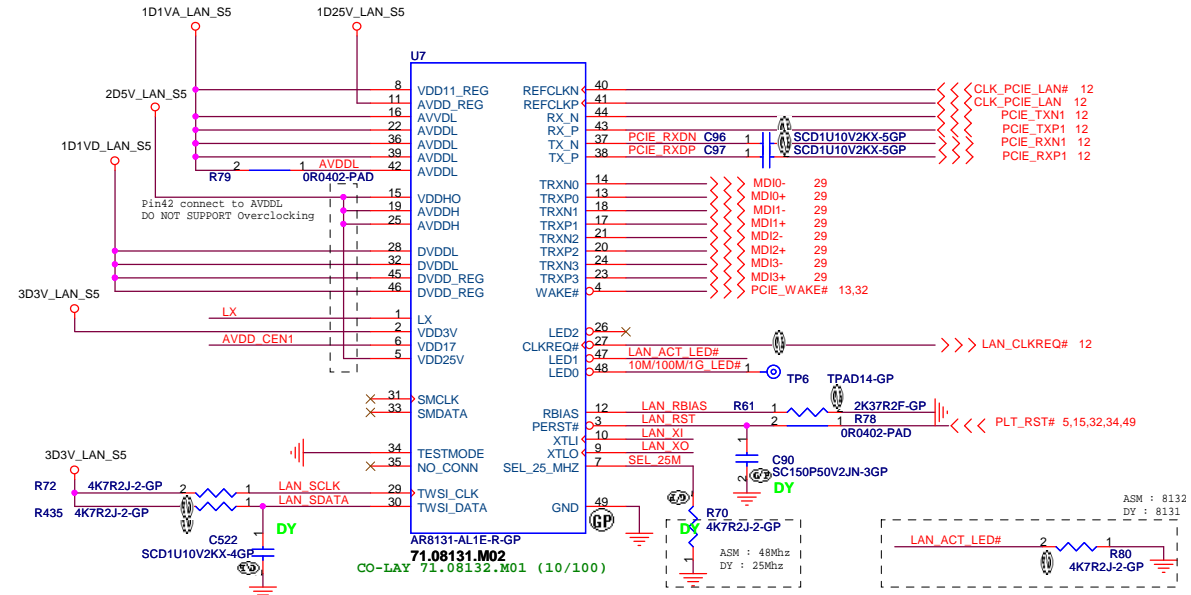
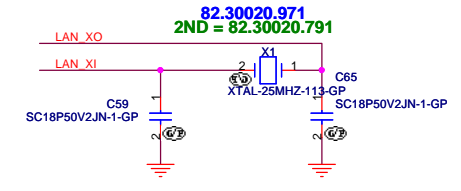
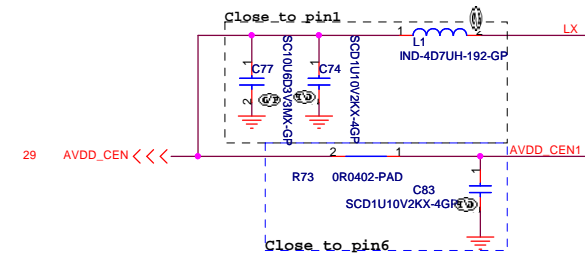
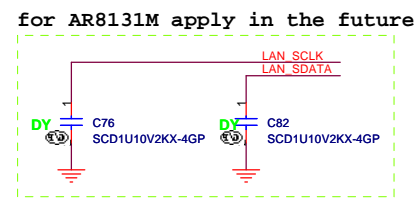
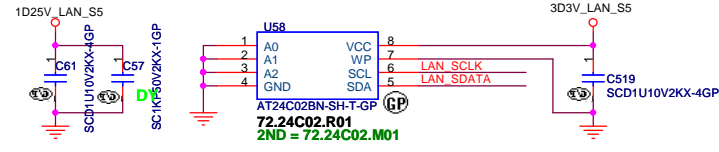
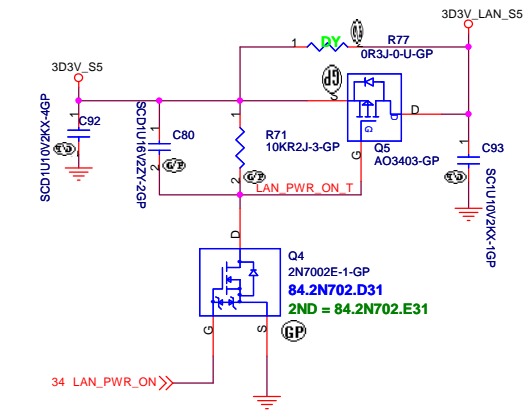
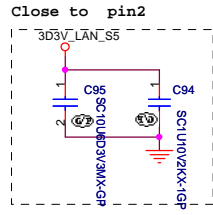
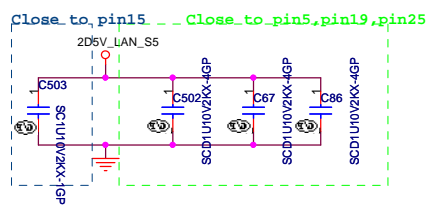
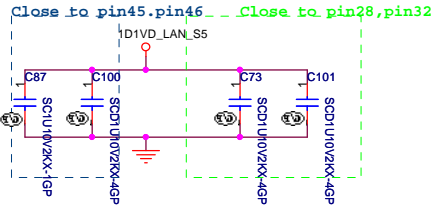
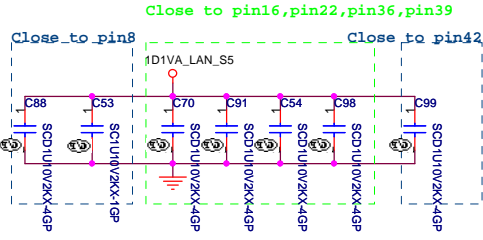
Bluetooth Power



BT CONN



<Variant Name>



<Variant Name>

緯創資通 Wistron Corporation

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Title

LAN AR8131/8132

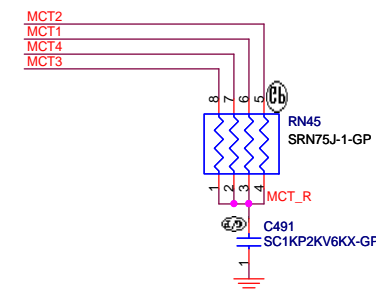
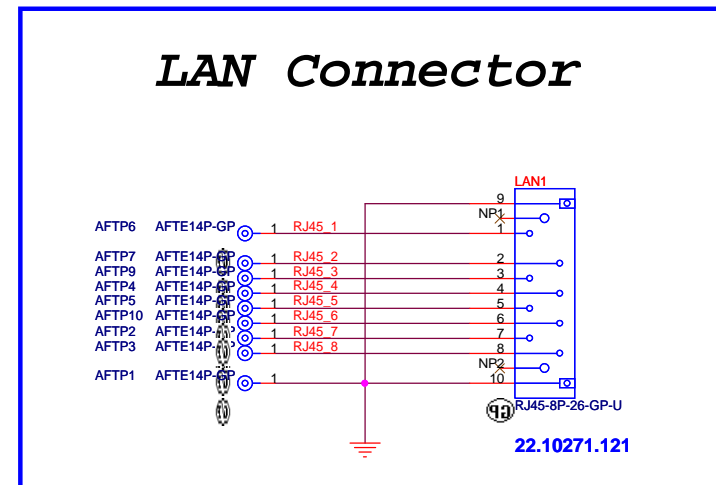
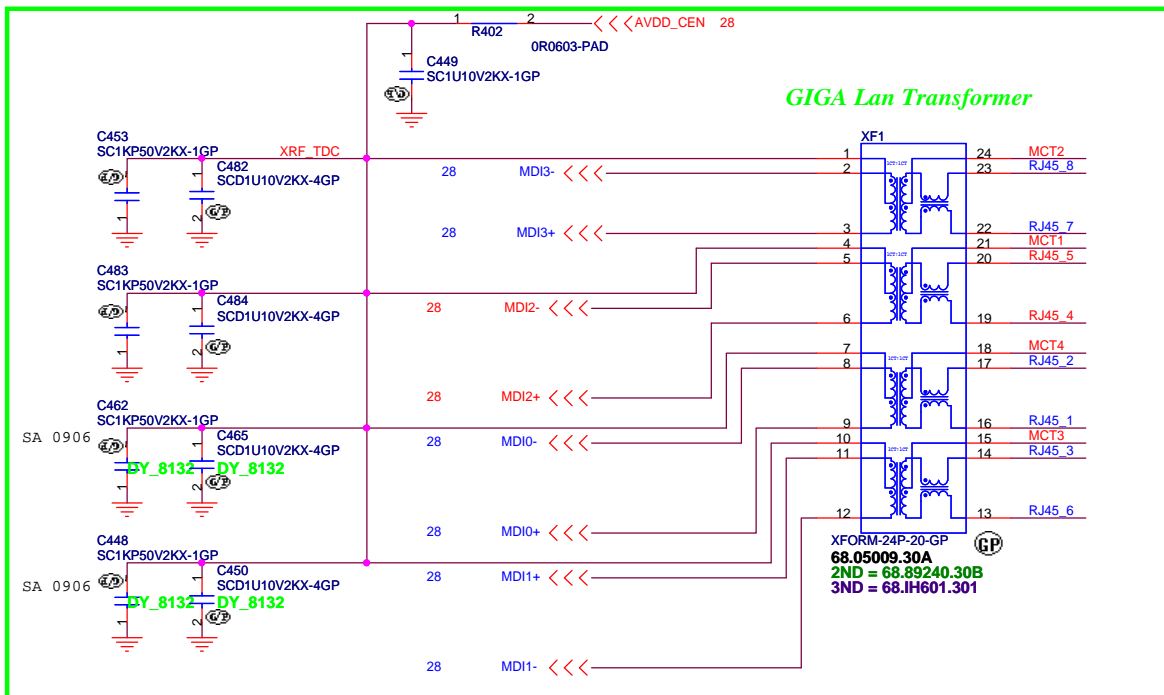
Size A3 Document Number

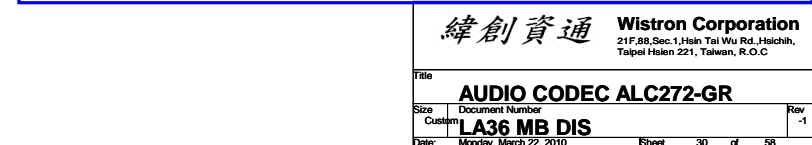
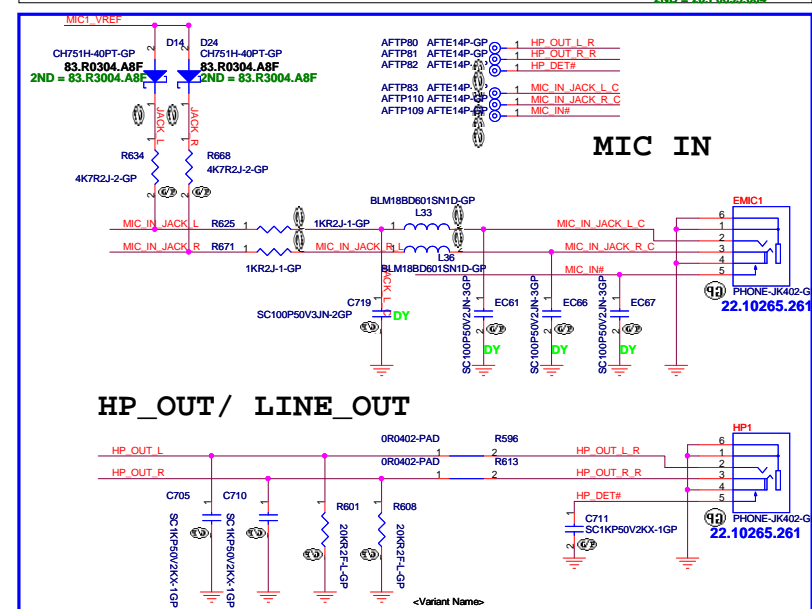
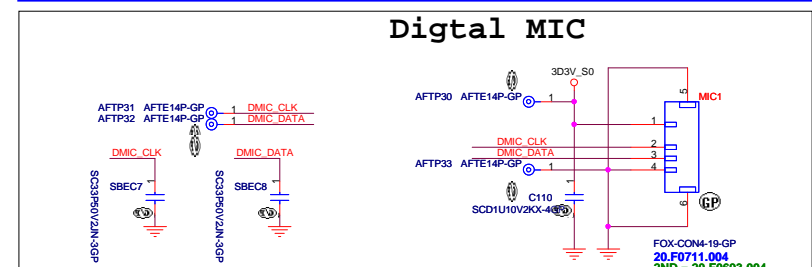
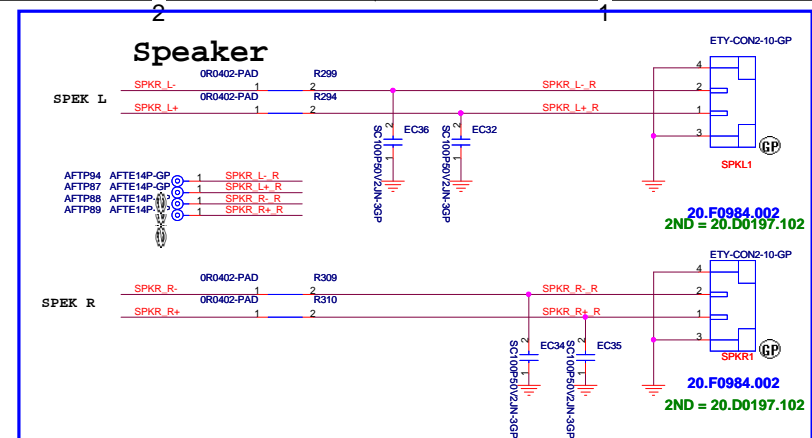
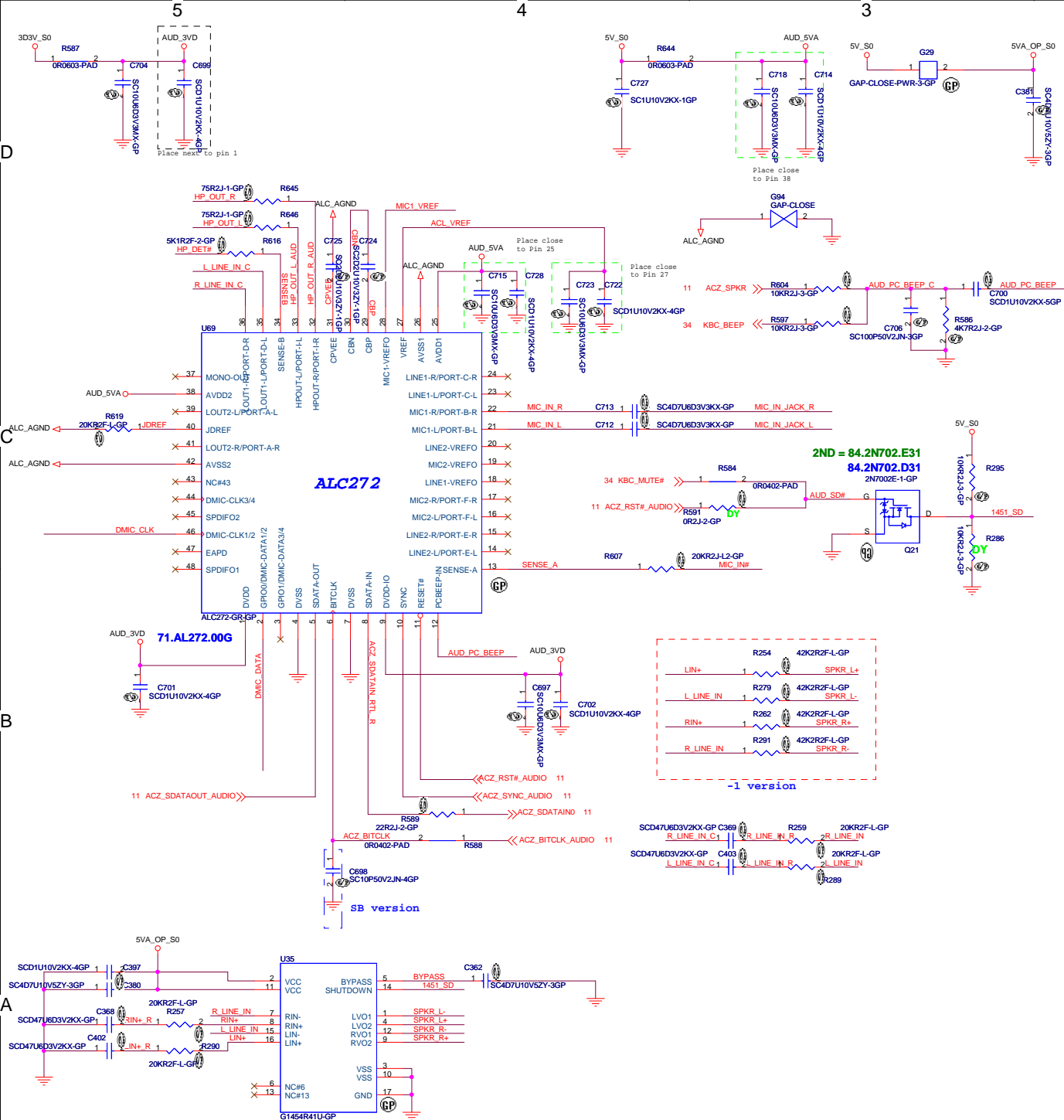
LA36 MB DIS

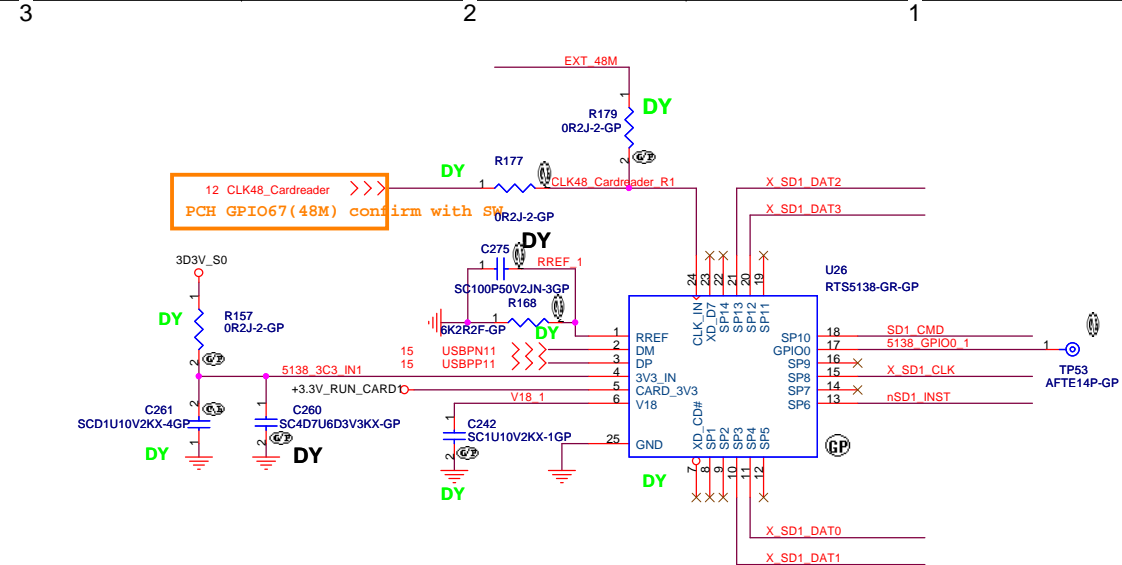
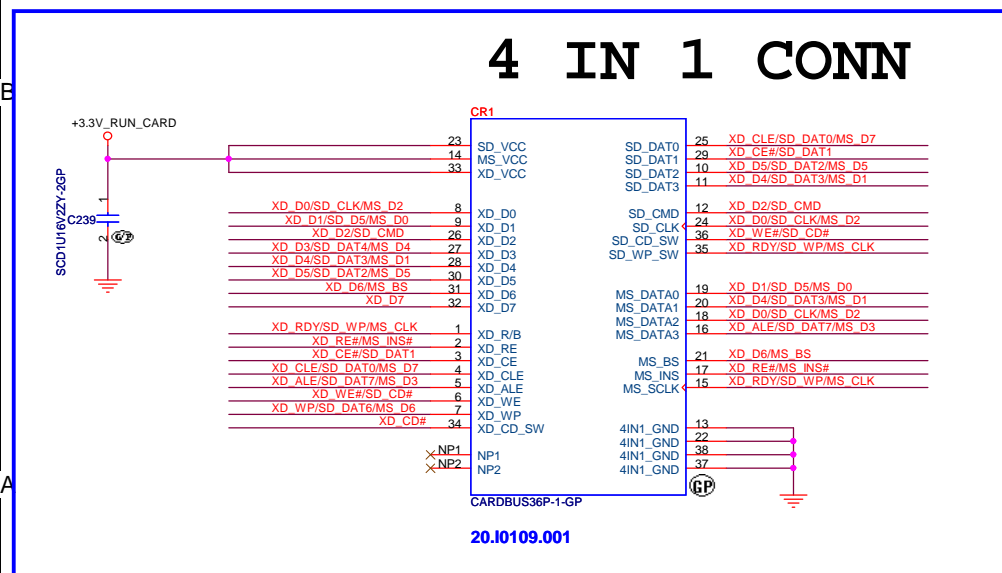
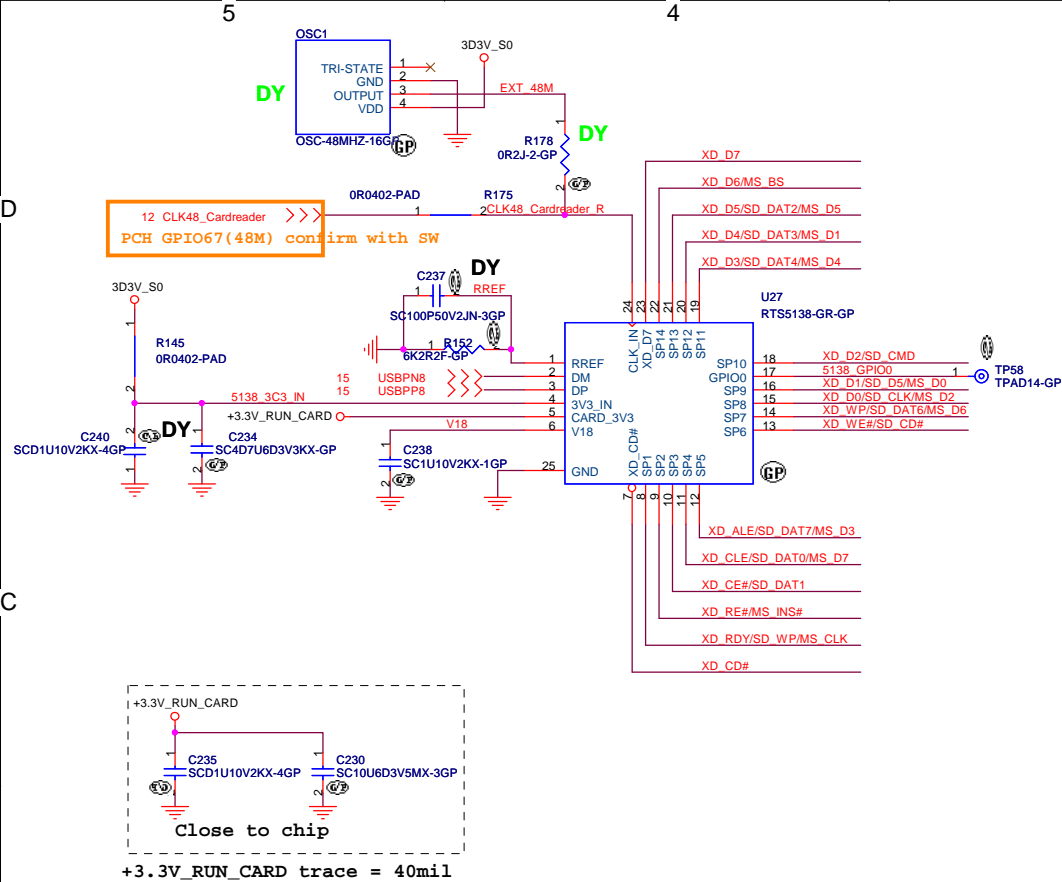
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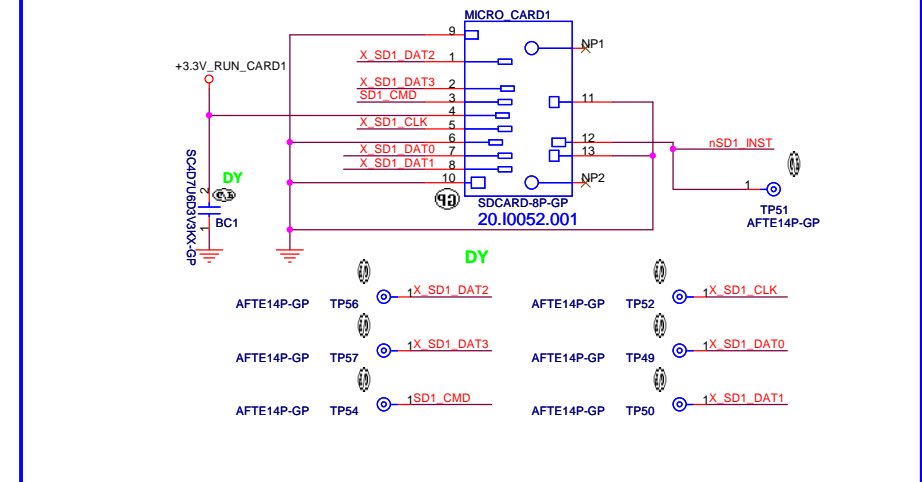
- 1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width, 12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except RJ-45 moat.







Micro SD CONN



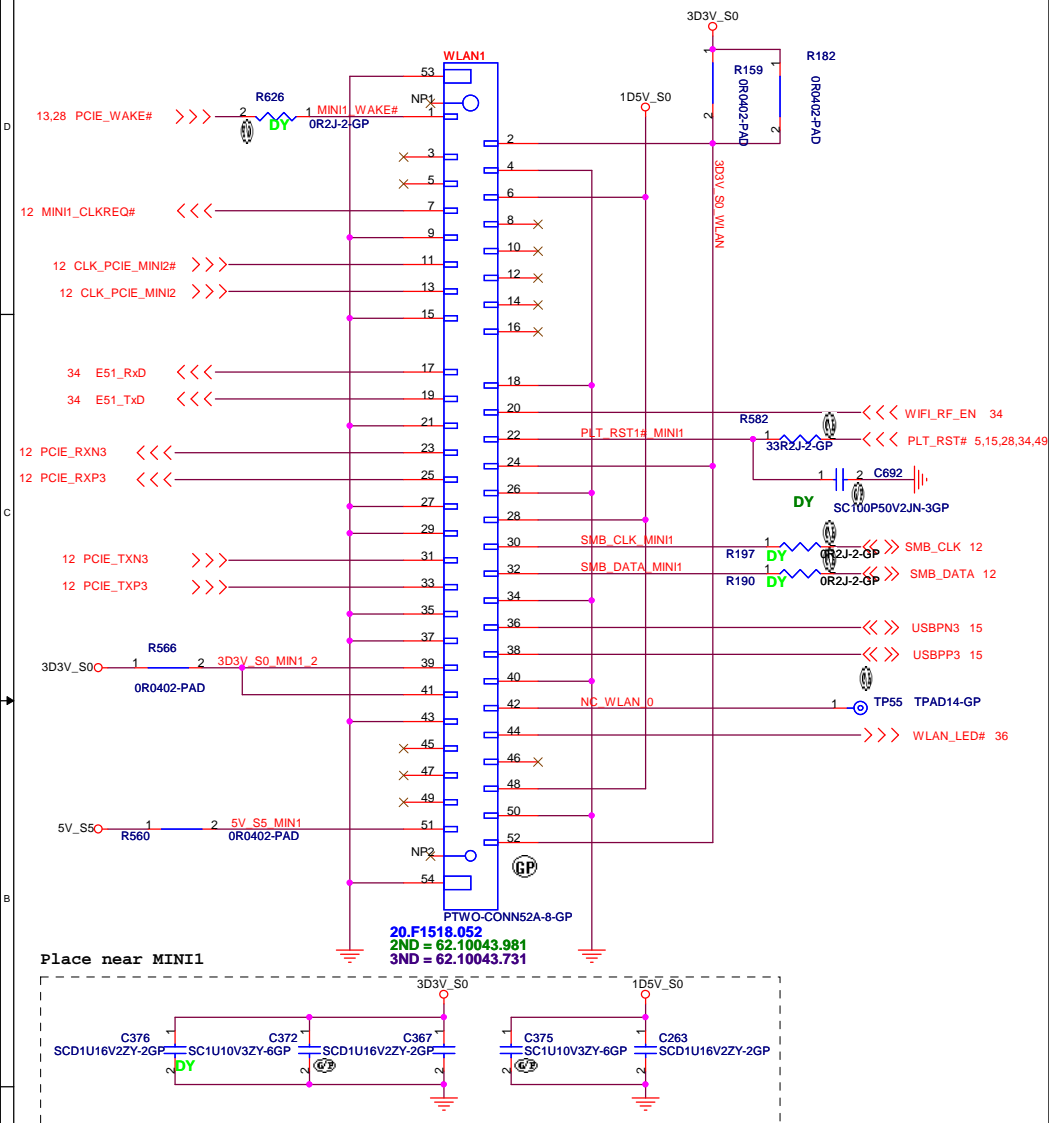
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緯創資通 Wistron Corporation

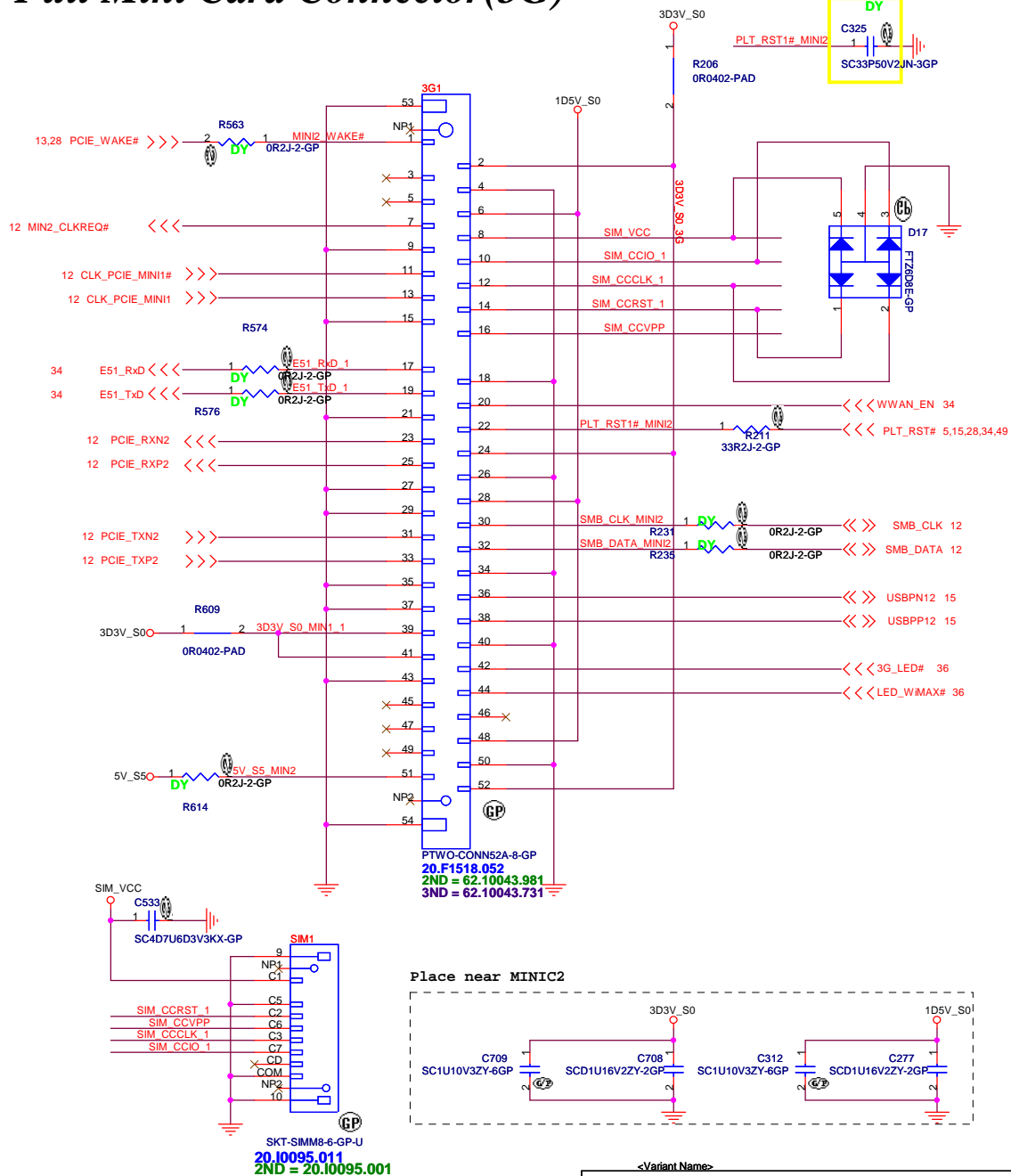
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

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Half Mini Card Connector(WLAN)



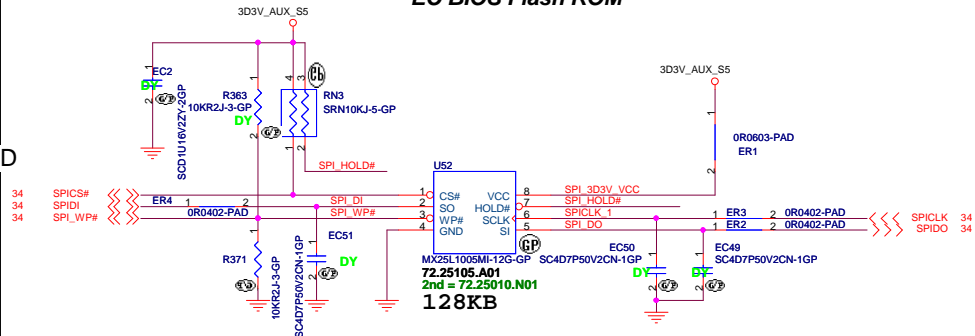
Full Mini Card Connector(3G)



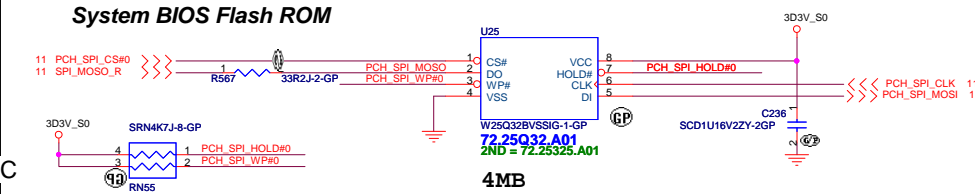
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緯創資通		Wistron Corporation	
21F,88,Sec.1,Hsin Tai Wu Rd.,Hsichih, Taipei Hsien 221, Taiwan, R.O.C			
Title			
MINI CARD			
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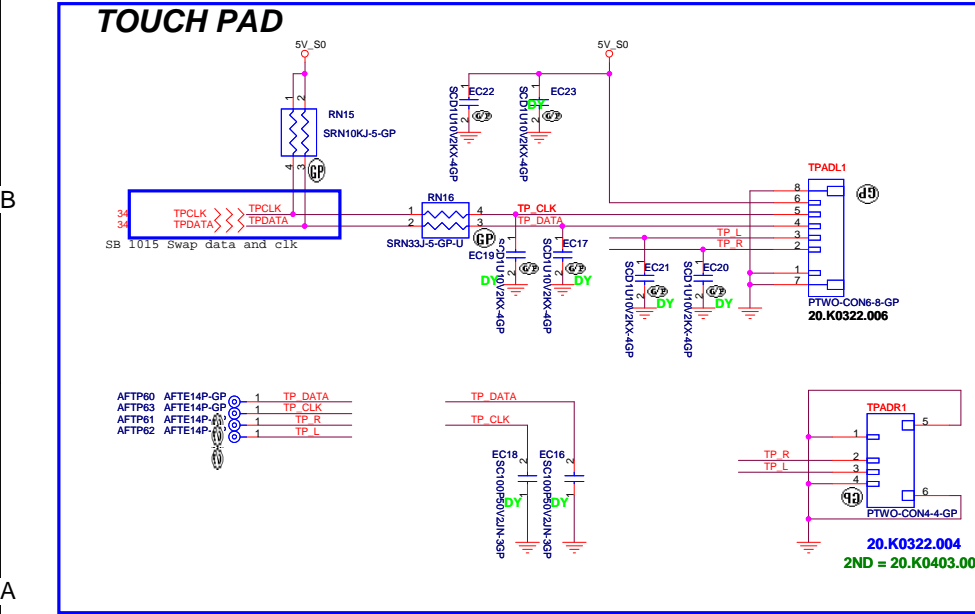
EC BIOS Flash ROM



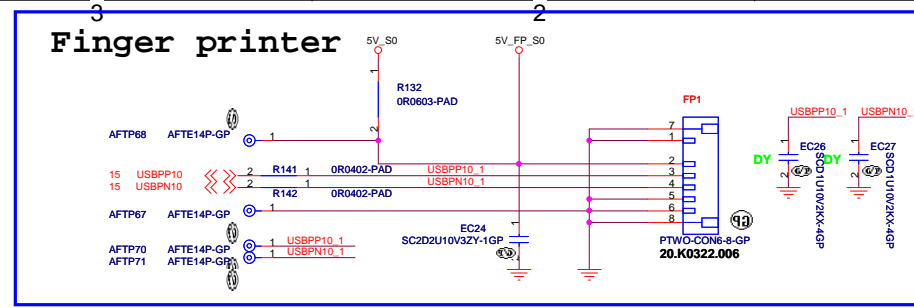
System BIOS Flash ROM



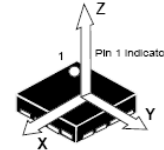
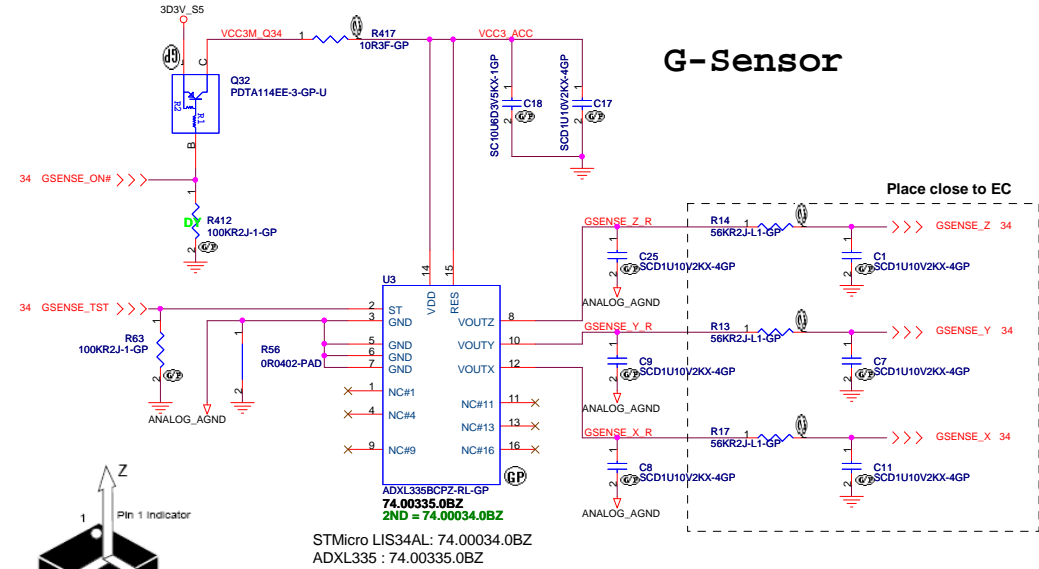
TOUCH PAD



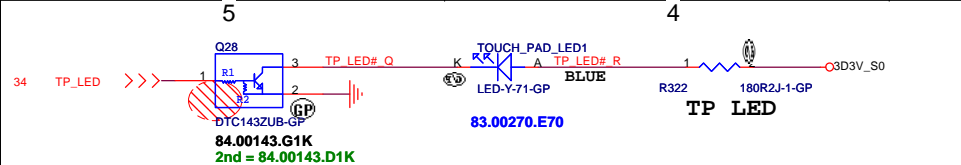
Finger printer



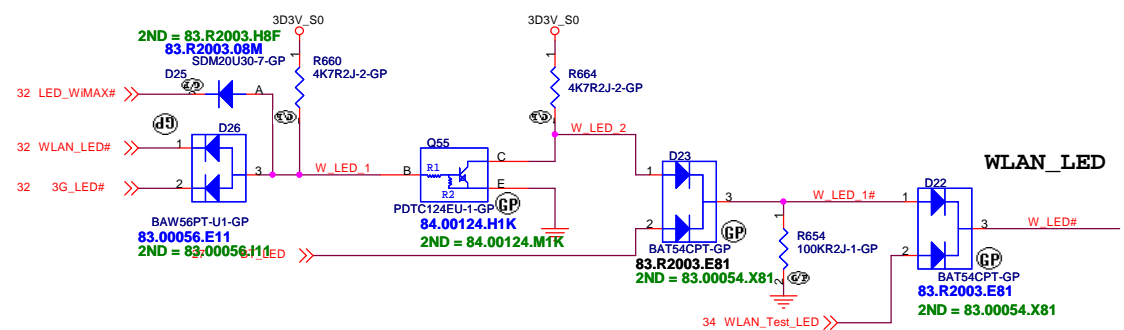
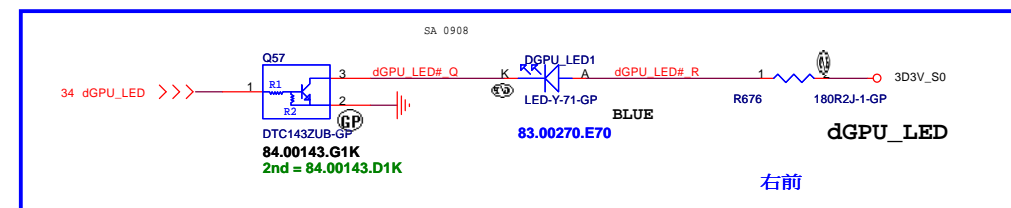
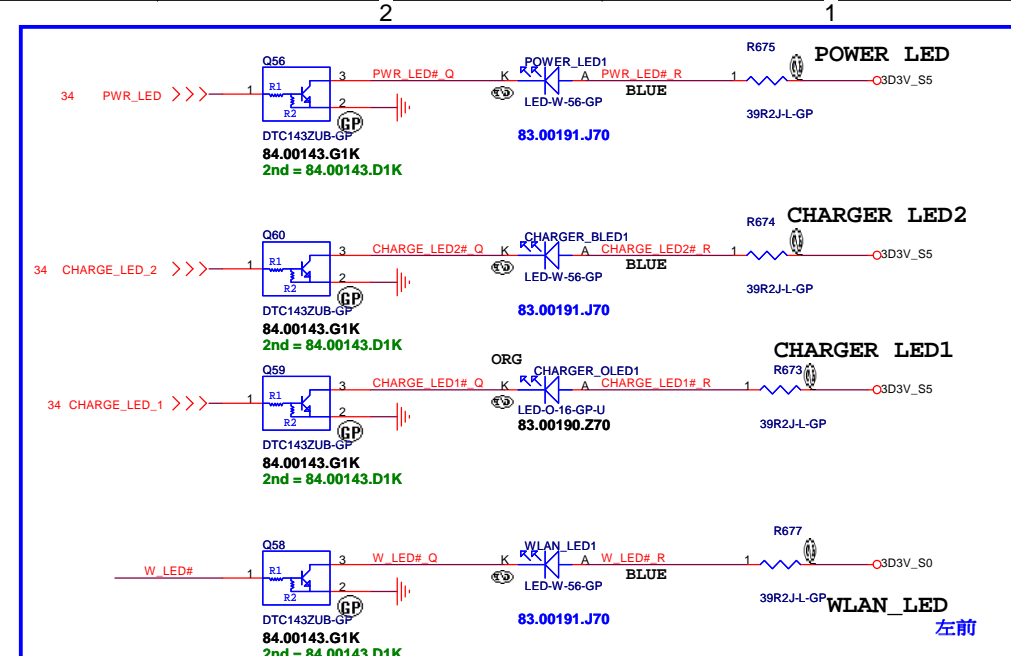
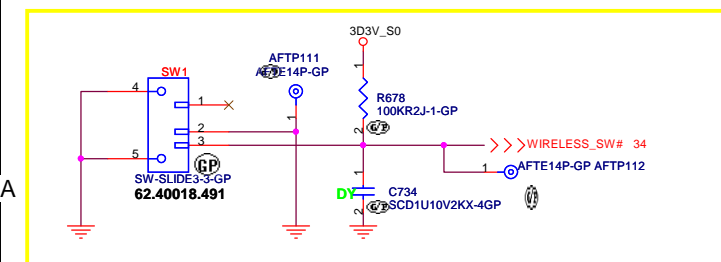
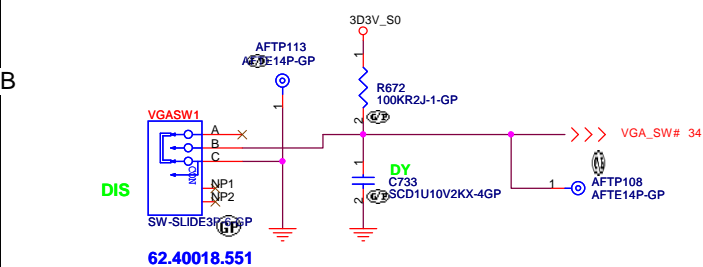
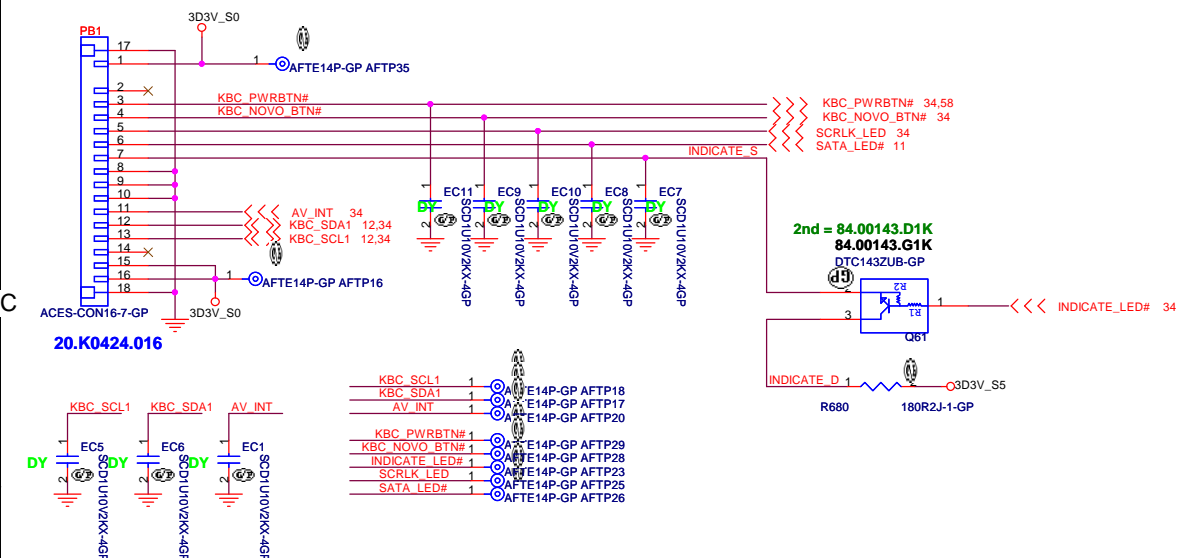
G-Sensor



<Variant Name>



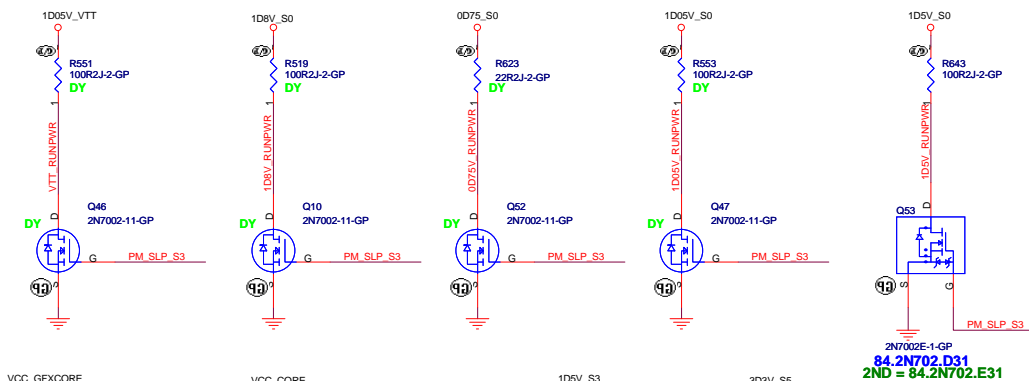
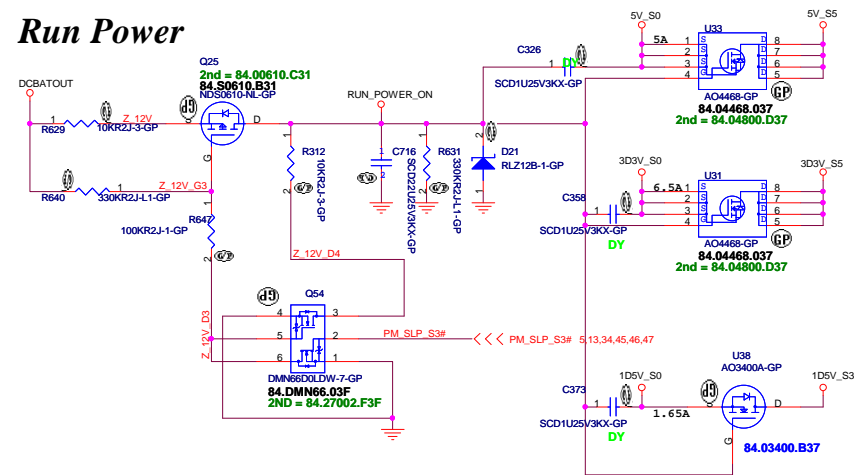
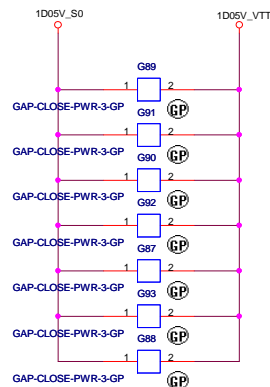
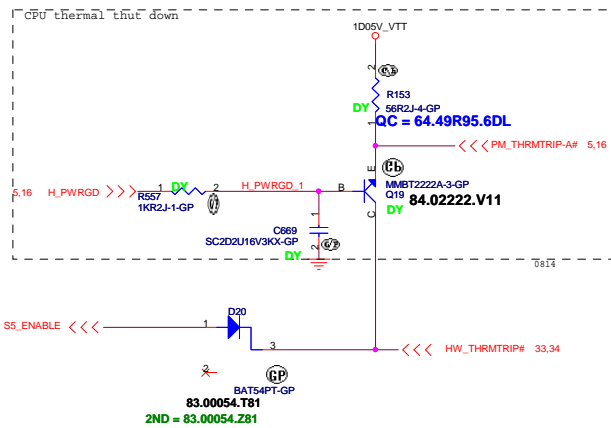
POWER BOARD CONN



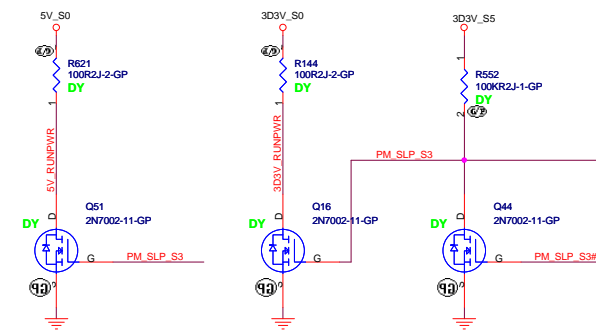
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緯創資通 Wistron Corporation
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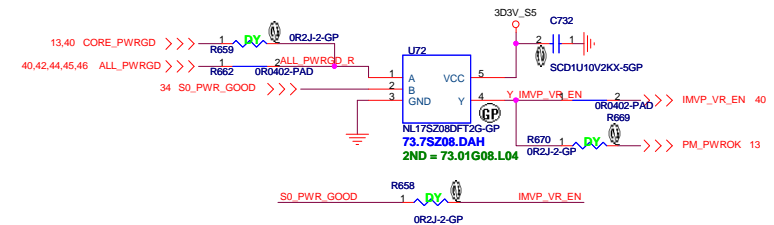
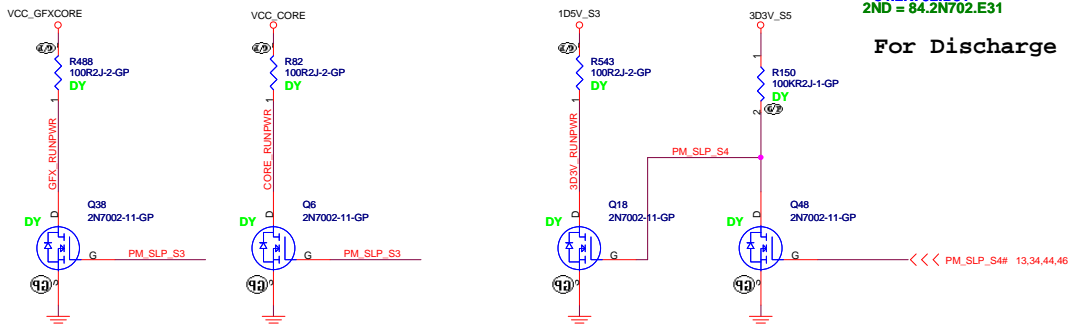
LED POWERBD CONN		
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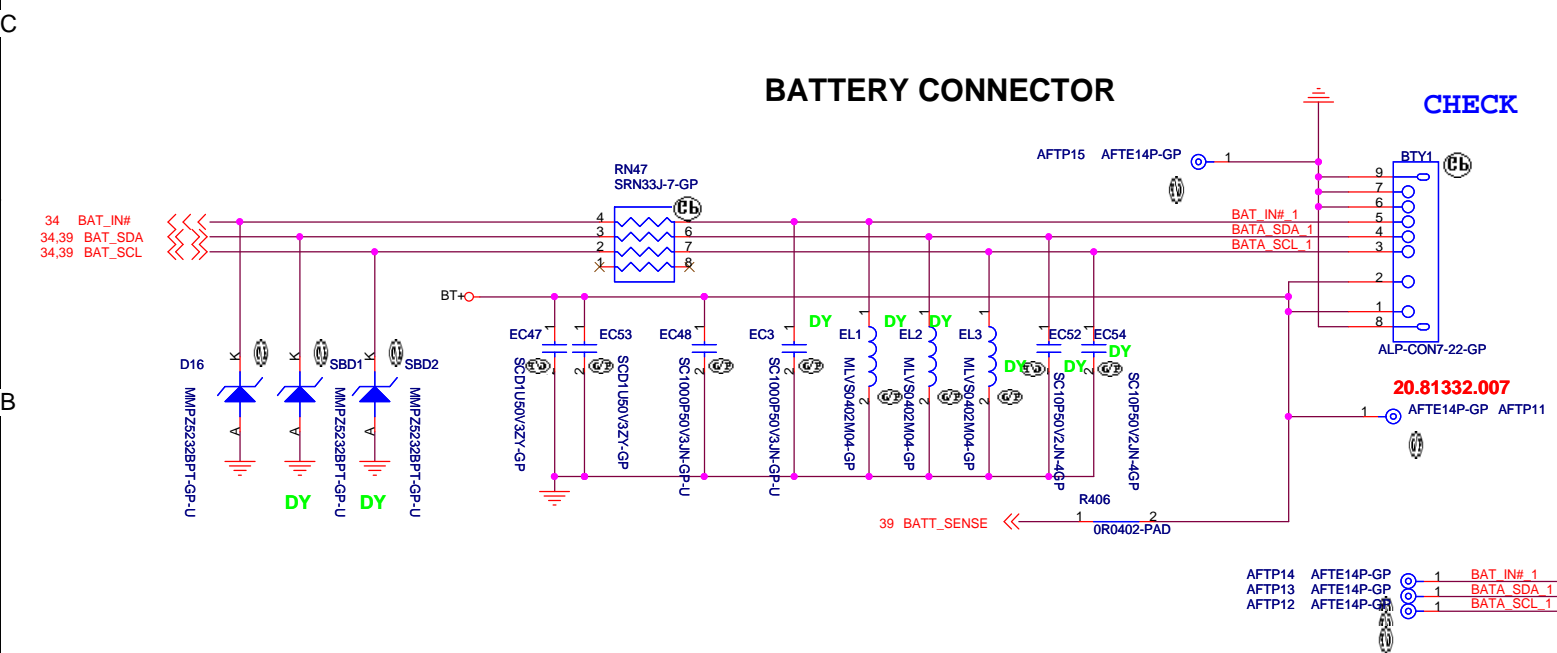
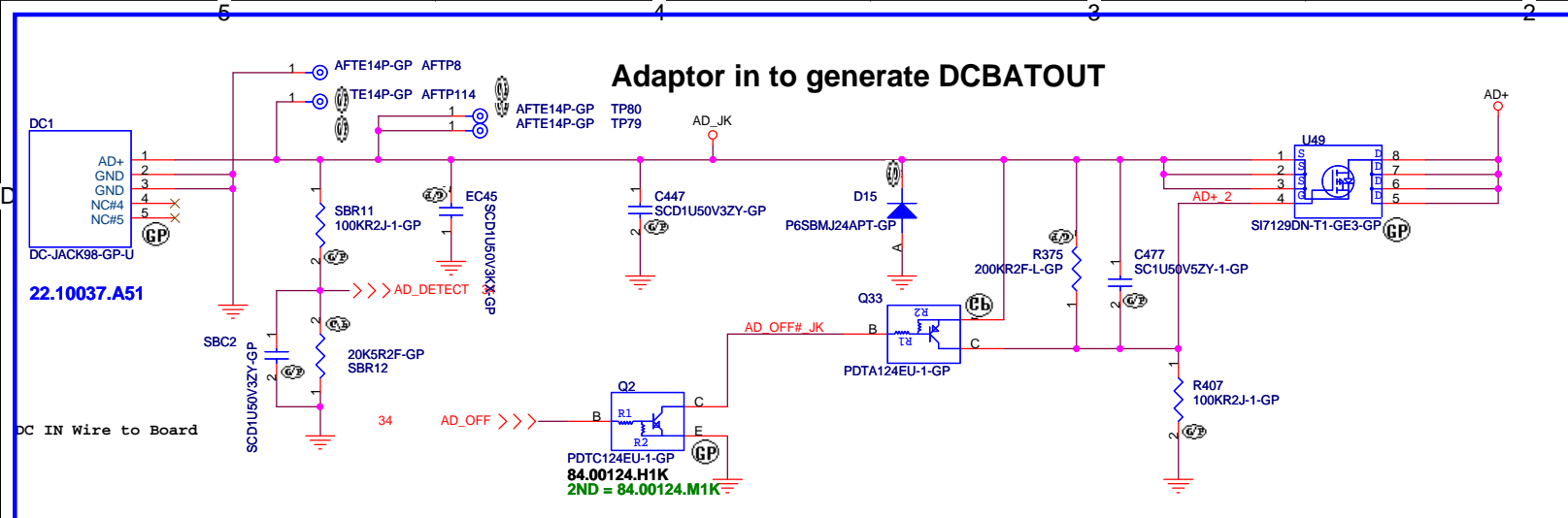


For Discharge

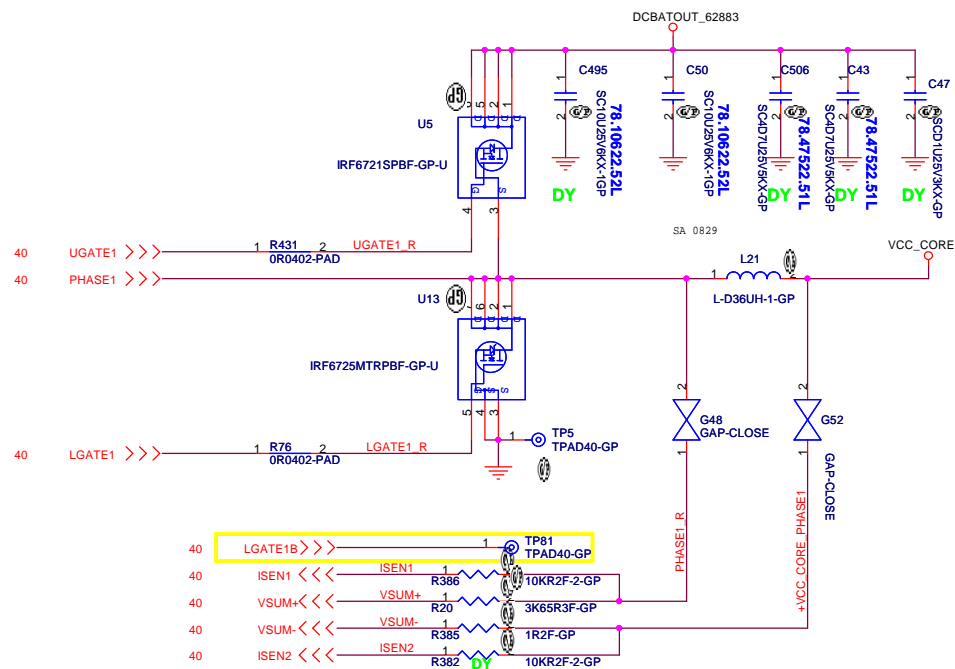
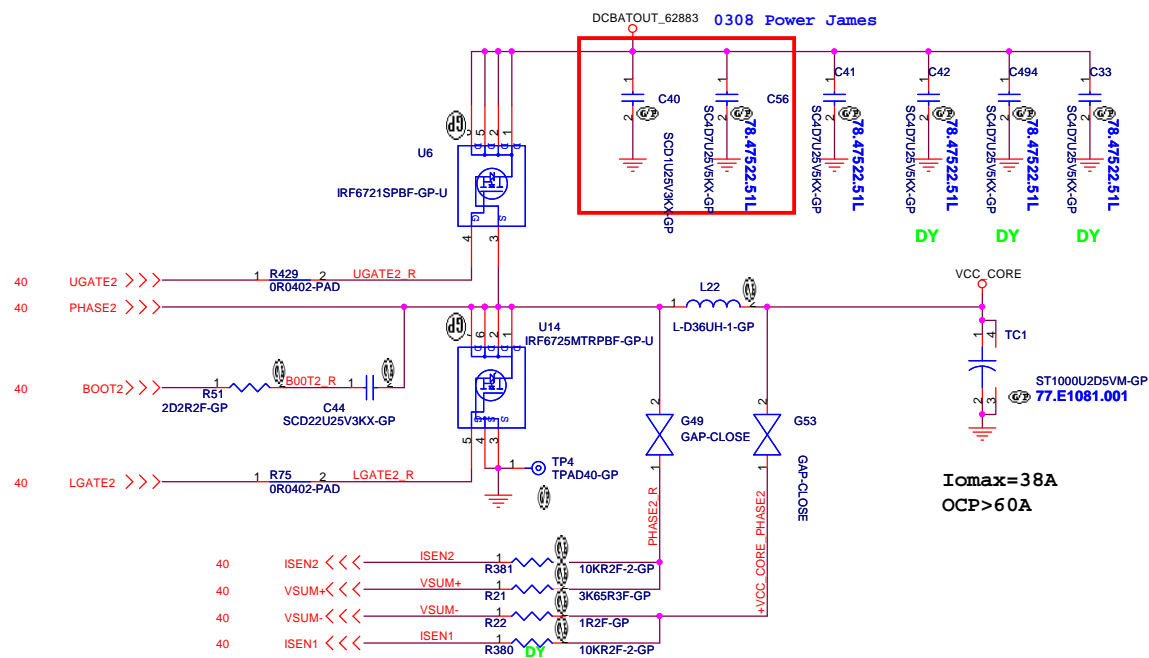


For Discharge

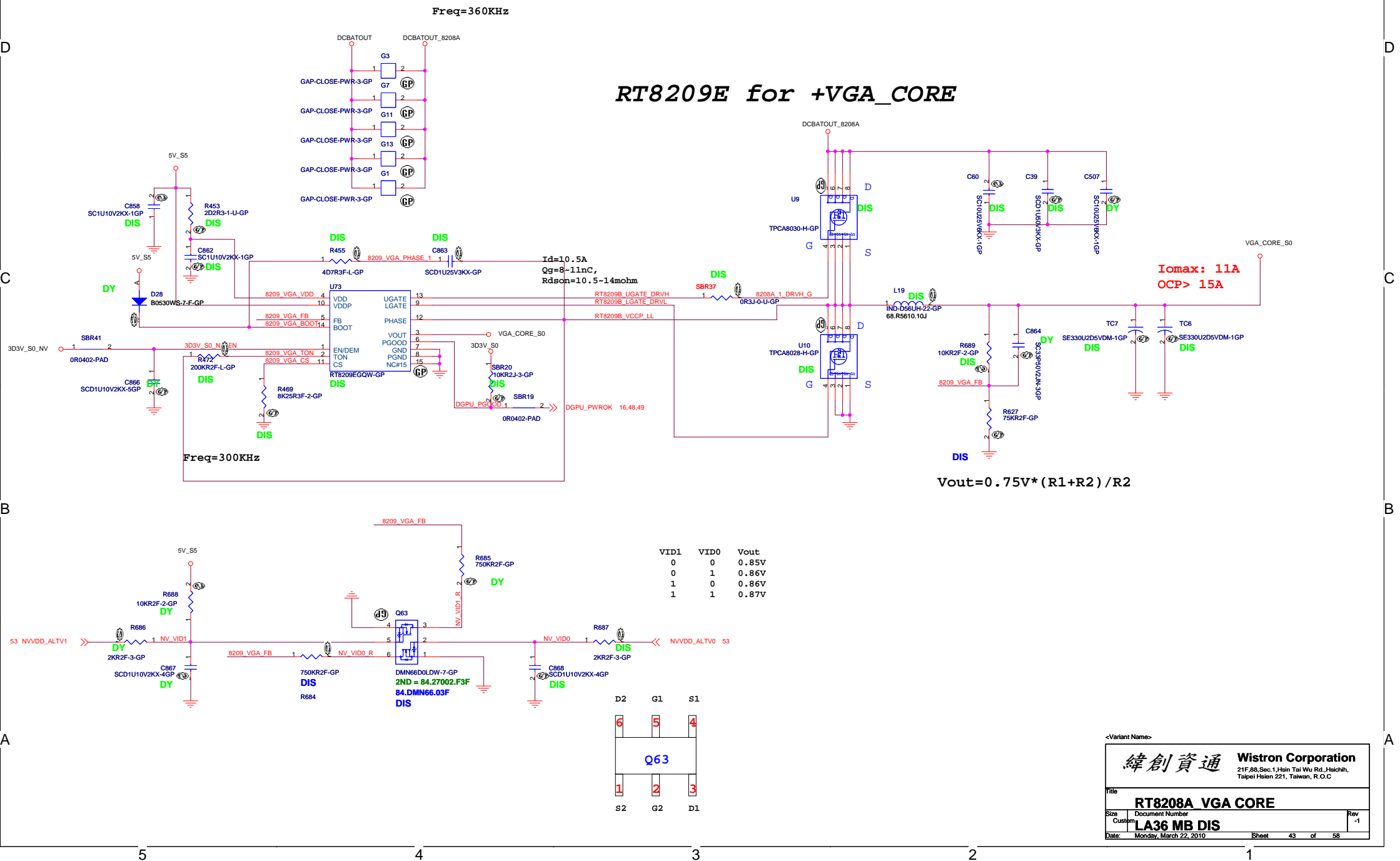




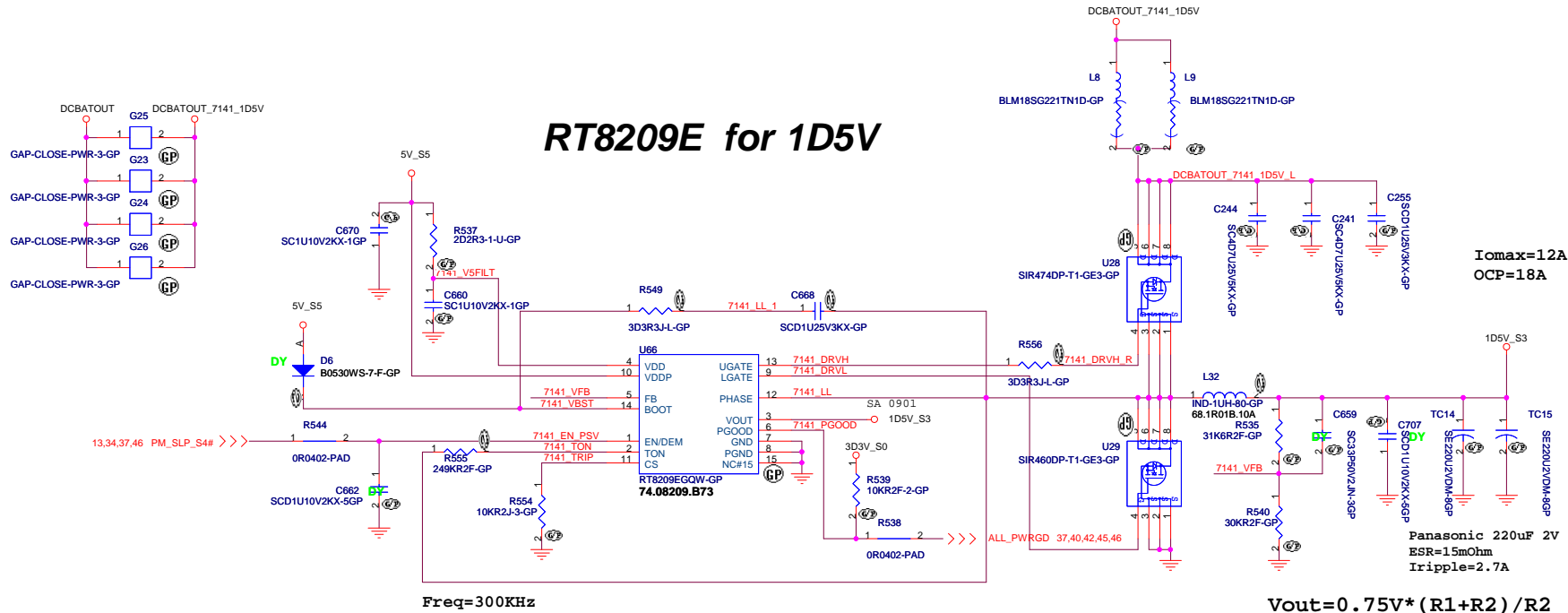




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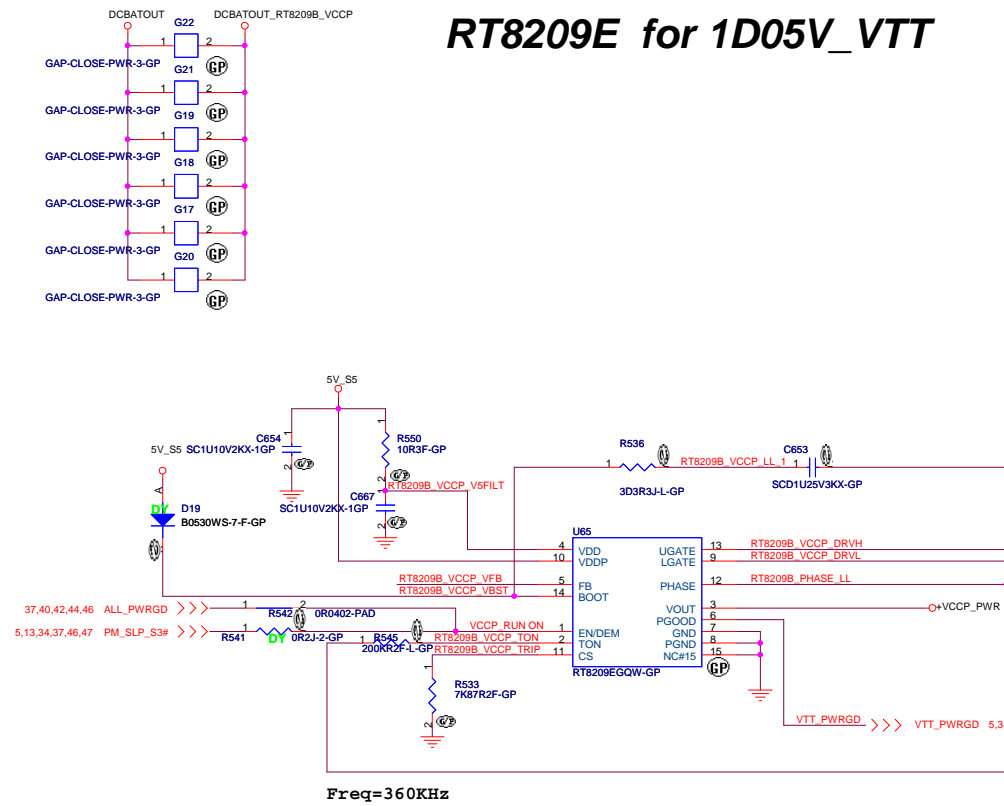


RT8209E for 1D5V

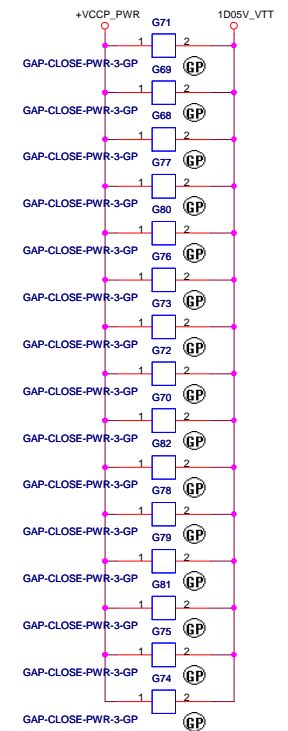
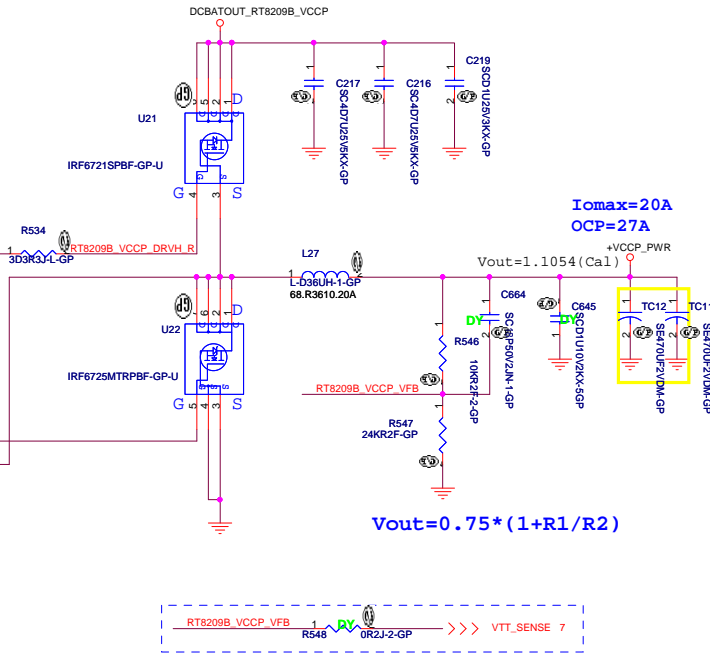


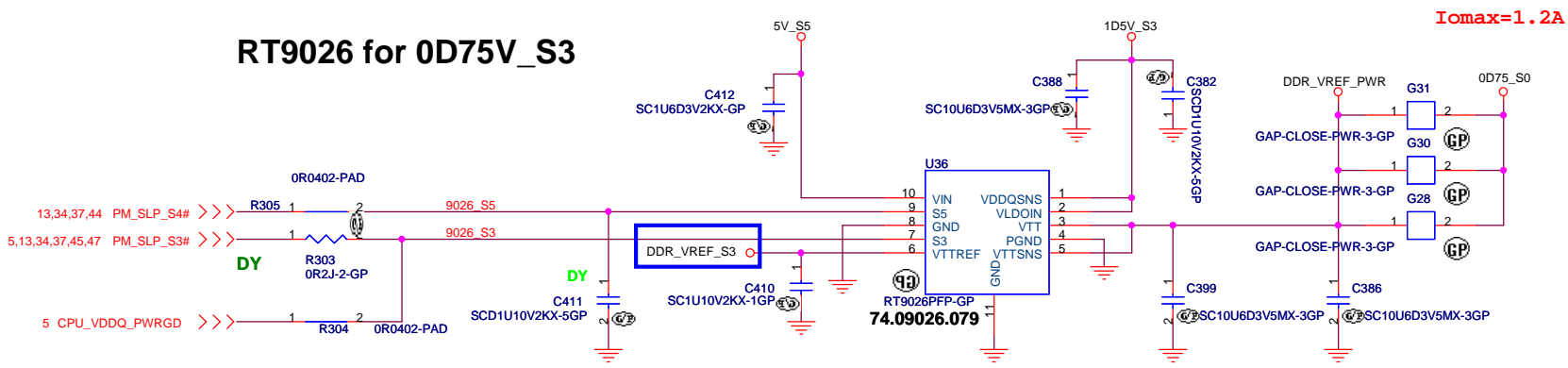
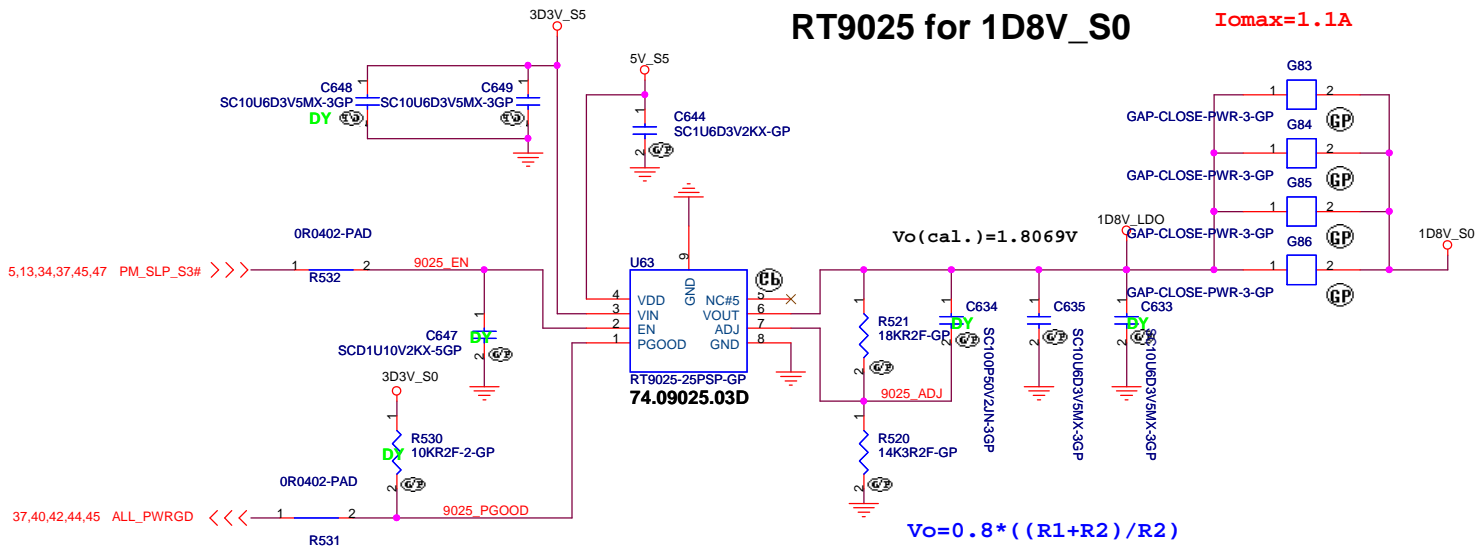
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緯創資通 Wistron Corporation			
21F,88,Sec.1,Hsin Tai Wu Rd.,Heichih, Taipei Hsien 221, Taiwan, R.O.C			
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RT8209E for 1D05V_VTT



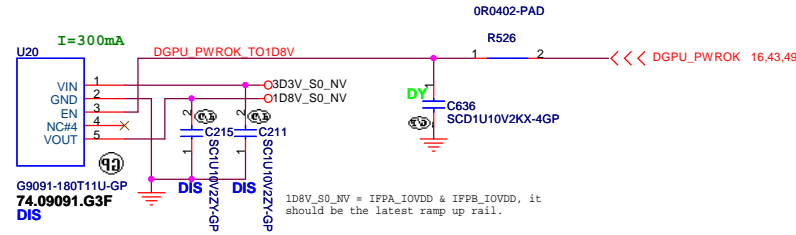
Freq=360KHz





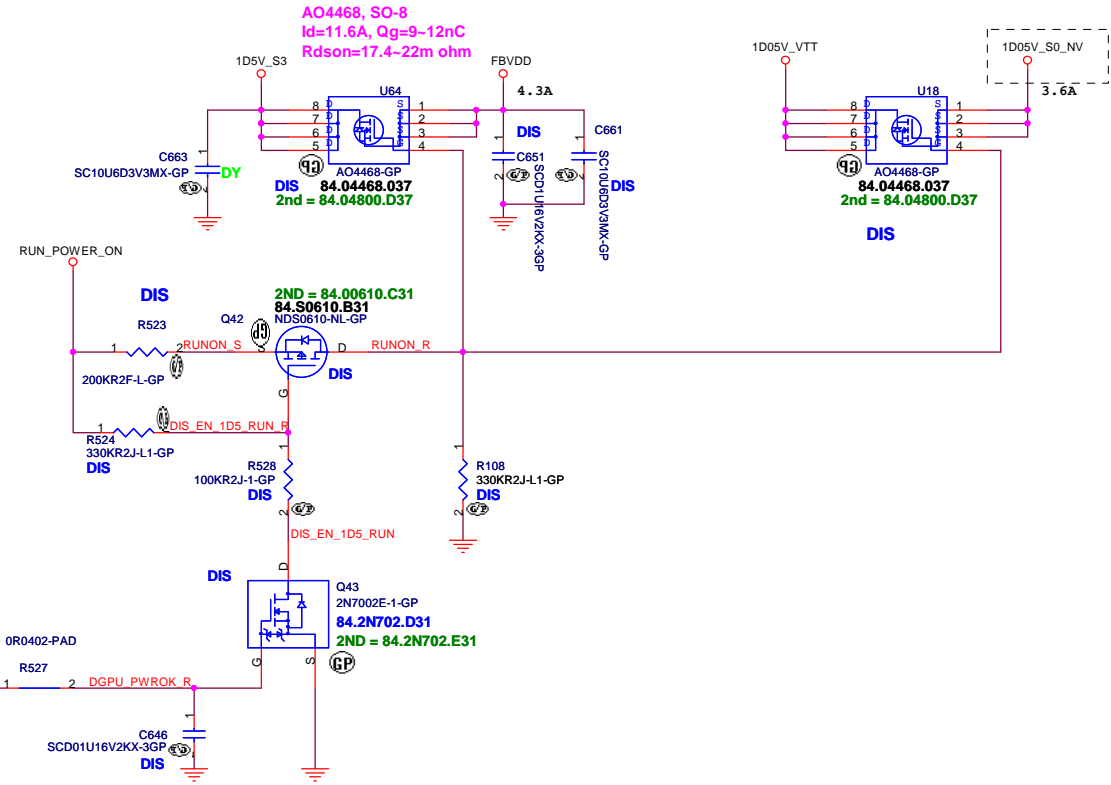
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21F.88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C		
Title		
RT9025 1D8V/ RT9026 0D75		
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+3VS to 1.8V Transfer



+1.5V to FBVDD Transfer

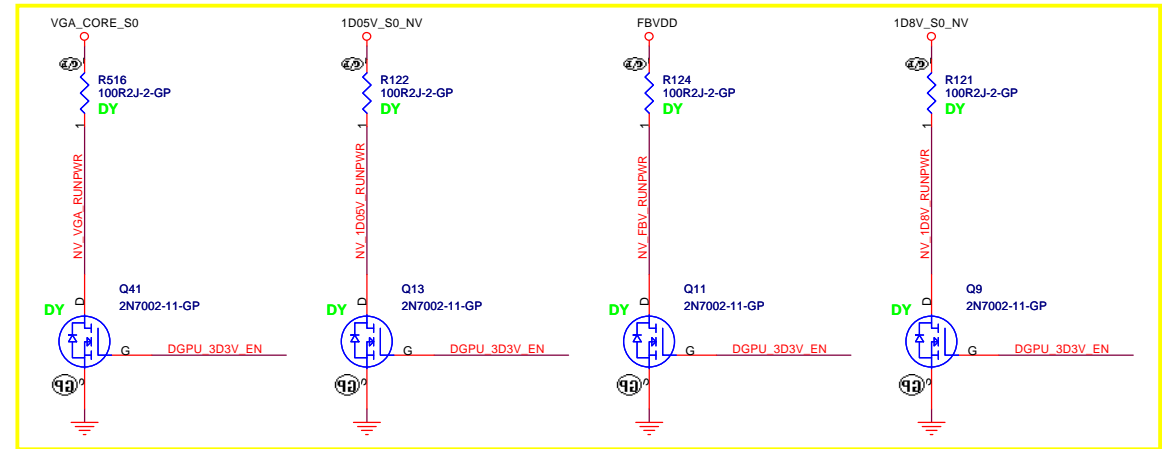
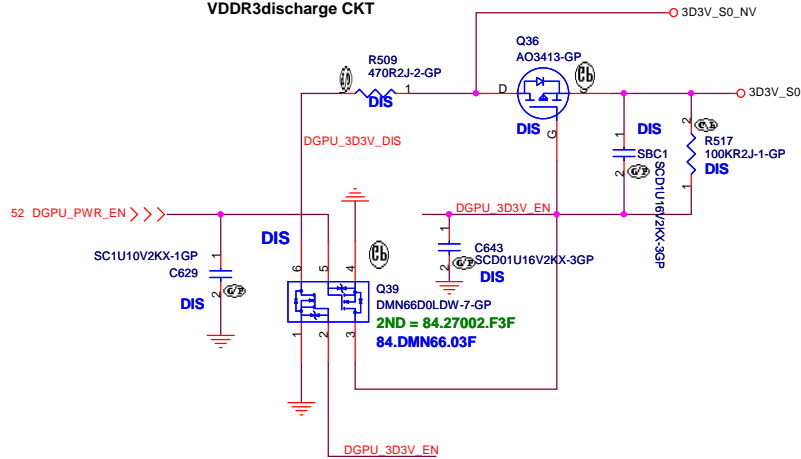
+1.05V to +1.05V_NV Transfer



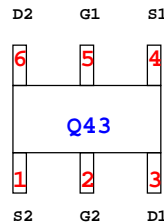
+3VS to 3.3V_DELAY Transfer

3.3v (580mA)

VDDR3discharge CKT

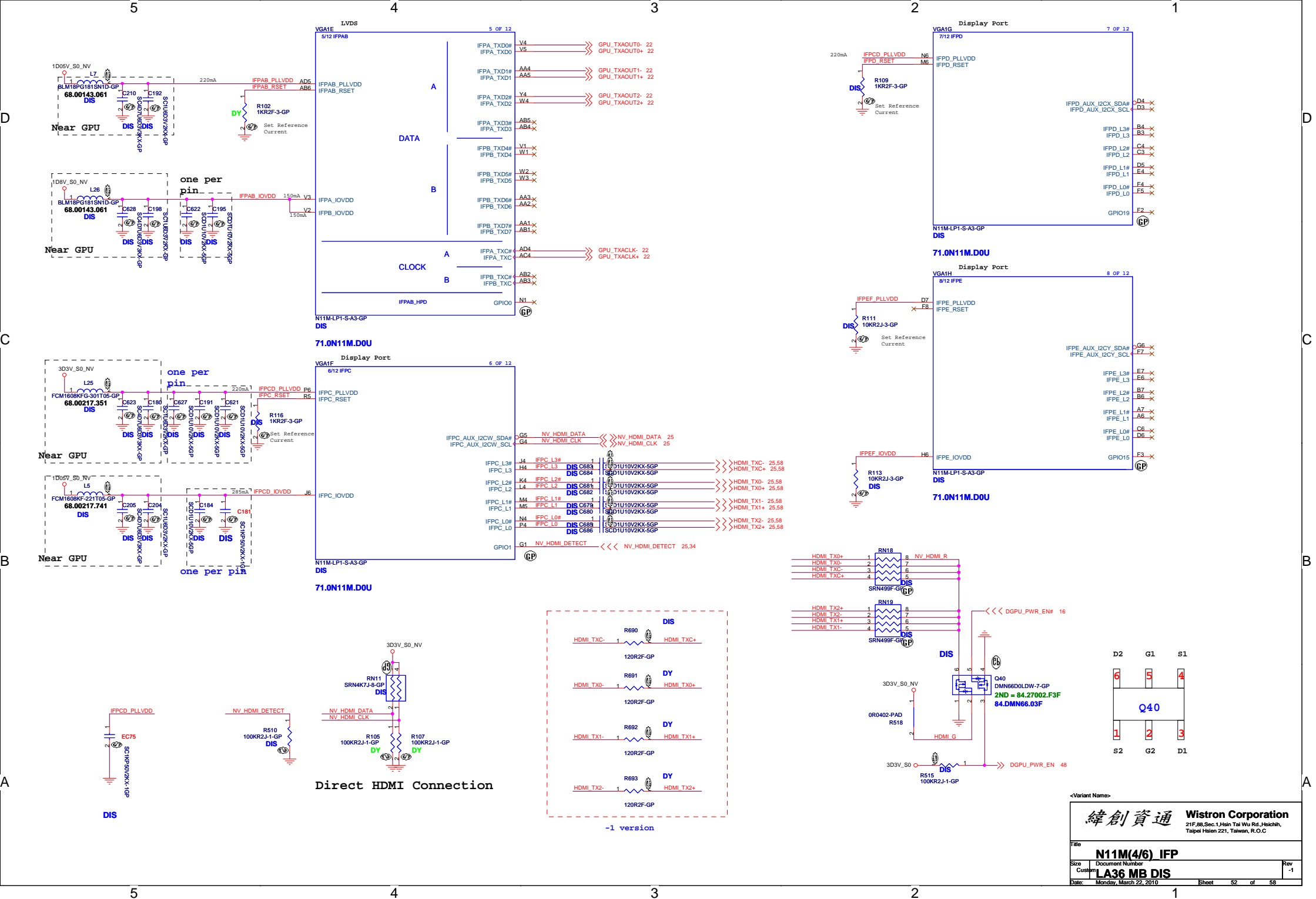


system turn on 3D3V_S0_NV --> VGA_CORE_S0
DGPU_PWROK --> FBVDD, 1D05V_S0_NV, 1D8V_S0_NV

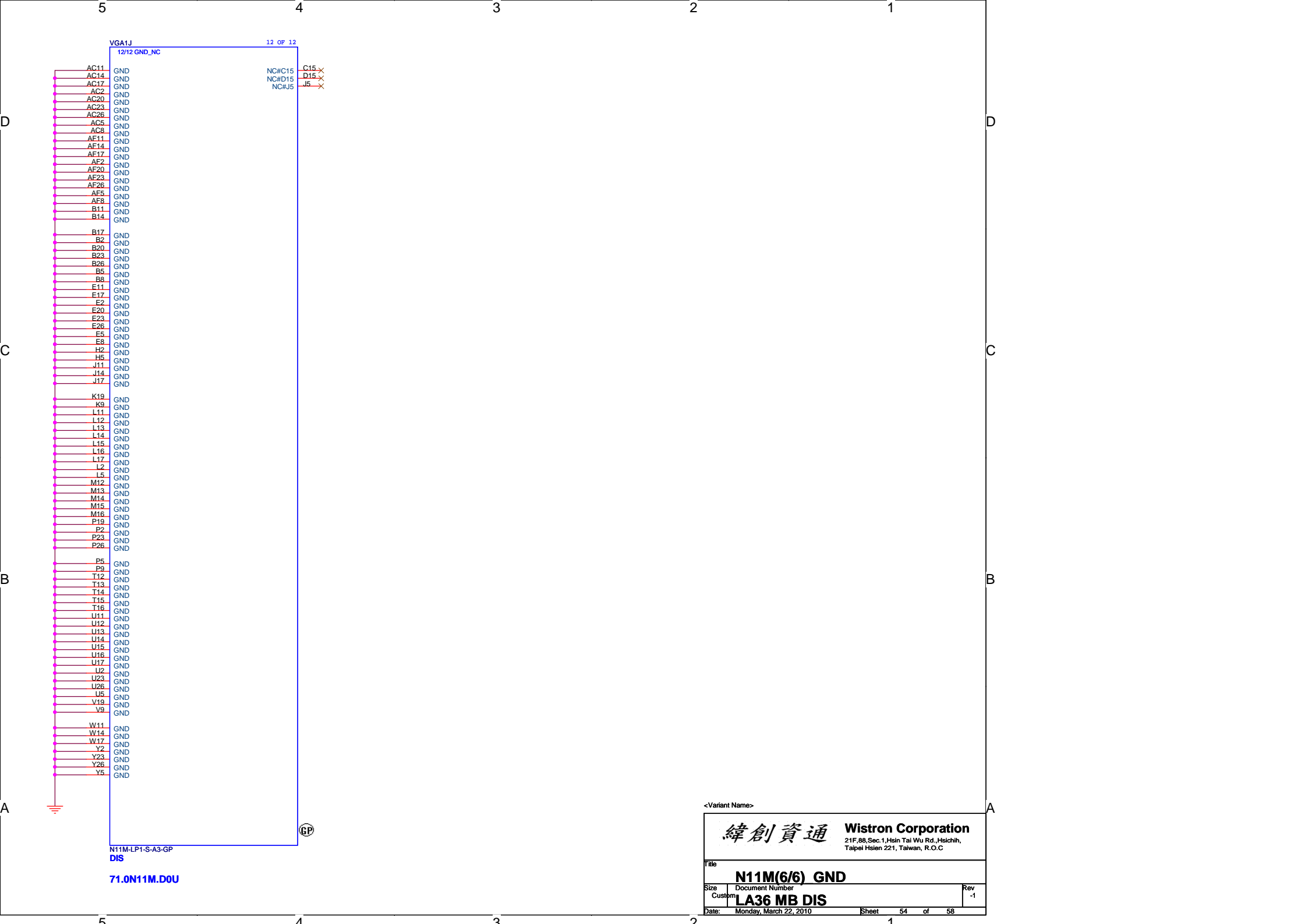


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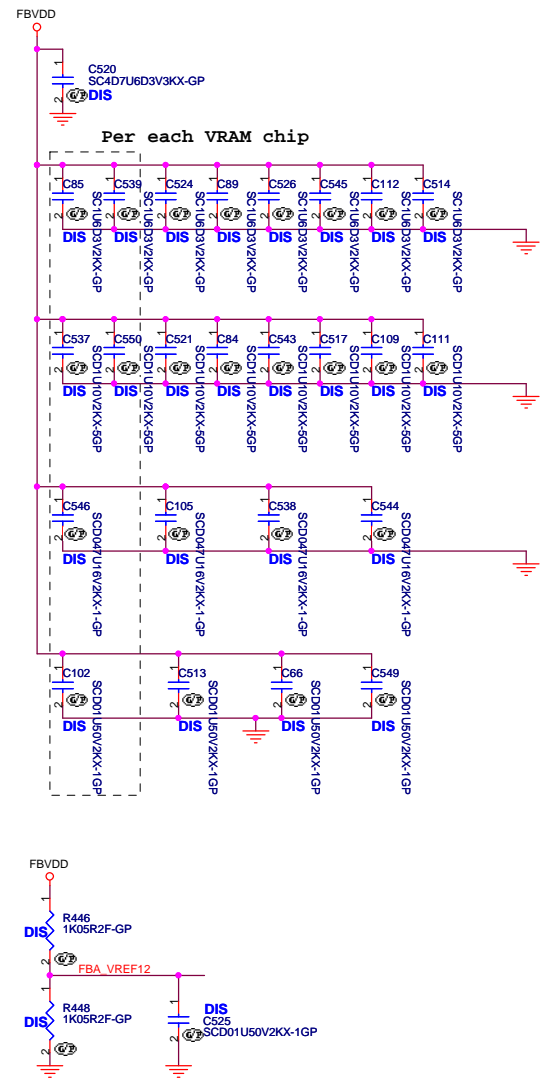
緯創資通		Wistron Corporation	
		21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C	
Title			
NV power			
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